ELECTRONICS FOR MEASUREMENT • COMPUTATION • TELEMETRY • CONTROL

INSTRUCTION MANUAL

for

PSK DEMODULATOR / PCM SYNCHRONIZER

MODEL GPD-6

DCS DATA-CONTROL SYSTEMS INC.

Instrumentation for Research

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PSL
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INSTRUCTION MANUAL

PSK DEMODULATOR/PCM SYNCHRONIZER

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DATA-CONTROL SYSTEMS, INC., EAST LIBERTY STREET, DANBURY, CONNECTICUT

INSTRUCTION MANUAL

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DOCUMENT NO: 680702 PUBLICATION DATE: 7/68

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Figure 1-1. PSK Demodulator/PCM Synchronizer, Model GPD-6.

SECTION I

DESCRIPTION AND LEADING PARTICULARS

1-1. GENERAL.

1-2. This handbook contains a general description, installation and operation instructions, and theory of operation for the Model GPD-6 PSK Demodulator/PCM Synchronizer, designed and manufactured by Data-Control Systems, Inc., East Liberty Street, Danbury, Connecticut.

1-3. Section I contains a general description including electrical and physical characteristics. Section II covers installation. Section III provides operating procedures. Section IV presents a complete theory of operation. Section V gives maintenance and troubleshooting procedures. Section VI contains engineering drawings of the Model GPD-6.

1-4. Material requiring clarification is illustrated with line drawings, halftones or listed in tabular form. The Model GPD-6 is illustrated in Figure 1-1.

1-5. PSK DEMODULATOR/PCM SYNCHRONIZER, MODEL GPD-6

1-6. An all-silicon, solid state laboratory instrument, the GPD-6 reconstructs clean data and a synchronous clock from PSK and PCM input data. One dual function switch selects all input codes and illuminates indicators to designate the type of input code to be processed, eliminating selection errors. The Model GPD-6 can operate in the following format code modes: PSK-NRZ-L, PSK-NRZ-M, PSK-NRZ-S, BIØ-L, BIØ-M, BIØ-S: NRZ-L, NRZ-M, NRZ-S and RZ. Output codes are selectable: NRZ-L with CLOCK or $\overline{\text{CLOCK}}$: RZ with CLOCK or $\overline{\text{CLOCK}}$. A square wave output PSK carrier can be used for further data processing or recording. The Model GPD-6 accepts input signals from receivers, tape recorders, wideband demodulators and similar source equipment.

1-7. All modes of operation require a plug-in bit rate tuning module, GPD-6/TU, which provides bit rate capabilities from 10 bps to 1,600,000 bps NRZ, or 5bps to 800,000bps RZ in 26 modules. To operate with PSK and BIØ codes, GPD-6/F plug-in modules are additionally required for carrier signals from 5Hz to 1.25MHz, or BIØ signals from 5bps to 1.25mbs. Separation of PSK from a multiplex is accomplished by an optional GPD-6/BP bandpass filter module. These plug-in units are listed in Table 1-1.

1-8. ELECTRICAL CHARACTERISTICS.

1-9. Bit synchronization with clock restoration is achieved using a Reference Loop for demodulation of PSK-NRZ and Bi-Phase and a Data Loop for PCM data. PSK and Bi-Phase signals are first processed in the Reference Loop and then in the Data Loop. PCM signals are processed in the Data Loop alone.

1-10. SPECIFICATIONS.

Input Impedance:	Greater than 10K ohms resistive at specified bit rates and signal levels and shunted by approximately 100pf.
Input Level:	0.5 volts to 25 volts peak-to-peak. No adjustments necessary.
Input Dynamic Range:	50:1. Sensitivity is extended down to 50mv peak-to-peak with the GPD-6/BP bandpass-amplifier. See Table 1-1.
Input Code Formats:	The following input code formats and modes are selectable by a front panel coaxial rotary switch: RZ, NRZ-L, NRZ-M, NRZ-S, Bi-Phase-M, Bi-Phase-S, PSK-NRZ-M, PSK-NRZ-L PSK-NRZ-S.
Carrier Frequency:	5Hz to 1.25MHz.
Bit Rate:	10bps to 1.6MBPS NRZ, 5BPS to 800 KB RZ and to 1.25MBPS Bi-Phase.
Bit Rate Selection:	Bit Rate ranges are selected by plug-in tuning units, Model GPD-6/TU. See table for bit rate range. Bit rate is continuously adjustable over the range indicated for each tuning unit. Any bit rate may modulate any carrier of the same or higher frequency in the PSK format.
Rise/Fall Time:	40 nanoseconds maximum, 10% to 90%.

Table 1-1. Plug-In Units

GPD-6/F Frequency Selector Units
(Necessary for all PSK and BIØ codes)

	Type No.	Lower Frequency	Upper Frequency
All Double Size Module	1	5 Hz	8 Hz
	2	8 Hz	12.5 Hz
	3	12.5 Hz	20 Hz
	4	20 Hz	32.5 Hz
	5	32.5 Hz	50 Hz
	6	50 Hz	80 Hz
	7	80 Hz	125 Hz
	8	125 Hz	200 Hz
	9	200 Hz	325 Hz
	10	325 Hz	500 Hz
	11	500 Hz	800 Hz
	12	800 Hz	1.25 kHz
	13	1.25 kHz	2 kHz
	14	2 kHz	3.25 kHz
	15	3.25 kHz	5 kHz
	16	5 kHz	8 kHz
	17	8 kHz	12.5 kHz
	18	12.5 kHz	20 kHz
	19	20 kHz	32.5 kHz
	20	32.5 kHz	50 kHz
	21	50 kHz	80 kHz
	22	80 kHz	125 kHz
	23	125 kHz	200 kHz
	24	200 kHz	325 kHz
	25	325 kHz	500 kHz
	26	500 kHz	800 kHz
	27	800 kHz	1.25 MHz

GPD-6/TU Bit Rate Selector Units
(Necessary for all PSK, BIØ, NRZ and RZcode

	Type No.	Lower Bit Rate (NRZ)*	Upper Rate (NRZ)*
Double Size Modules	1	10 bps	16 bps
	2	16 bps	25 bps
	3	25 bps	40 bps
	4	40 bps	65 bps
	5	65 bps	100 bps
Single Size Modules	6	100 bps	160 bps
	7	160 bps	250 bps
	8	250 bps	400 bps
	9	400 bps	650 bps
	10	650 bps	1 kbs
	11	1 kbs	1.6 kbs
	12	1.6 kbs	2.5 kbs
	13	2.5 kbs	4 kbs
	14	4 kbs	6.5 kbs
	15	6.5 kbs	10 kbs
	16	10 kbs	16 kbs
	17	16 kbs	25 kbs
	18	25 kbs	40 kbs
	19	40 kbs	65 kbs
	20	65 kbs	100 kbs
	21	100 kbs	160 kbs
	22	160 kbs	250 kbs
	23	250 kbs	400 kbs
	24	400 kbs	650 kbs
	25	650 kbs	1000 kbs
	26	1000 kbs	1600 kbs

*For RZ and Bi-Phase codes, divide listed bit rate by 2.

GPD-6/BP Band Pass Filter:
(Necessary to separate PSK signal from multiplex).

Order, stating carrier reference frequency, bit rate, code format and other multiplexed signals.

Standard Available: Carrier - 1.024 MHz; ±55kHz.

Gain Switchable	Maximum Input	Minimum Sensitivity
X1	7V PP	500 MV PP
X3	3V PP	170 MV PP
X10	1V PP	50 MV PP

1-11. PHYSICAL CHARACTERISTICS.

1-12. The Model GPD-6 is contained within a heavy wall, aluminum main case 8-1/2" x 19" x 20". The case contains a control module, ten synchronizer circuit boards, five power supply circuit boards, and seven front panel compartments for data plug-in tuning unit, PSK and Bi-Phase frequency selector unit and bandpass filter. The circuit boards are itemized in Table 1-2.

1-13. The control module mounts the two Reference Loop meters and SET push-button (lower left), the two Data Loop meters and SET pushbutton (upper left), concentric mode and format switches and corresponding mode and format lights, seven signal monitor jacks, power pushbutton and invert pushbutton.

1-14. A thumbhole in the GPD-6 top cover provides access to two toggle switches: RZ/NRZ-L DATA output switch and a CLOCK, $\overline{\text{CLOCK}}$ output switch.

1-15. A muffin fan is mounted on the rear of the GPD-6 to provide cooling.

1-16. CIRCUIT BOARDS.

1-17. Each circuit board is mounted and connected by Elco pins to the master board which is mounted on the main chassis.

1-18. TELEMETRY CODE FORMATS.

1-19. Code formats are illustrated in Figure 1-2.

1-20. PSK. The PSK carrier is phase modulated by PCM codes of the NRZ family. At every NRZ level change, the PSK carrier phase is shifted 180°: actually, the phase shifts alternate between ±90° of the carrier zero phase. When the carrier frequency is an integral multiple of the NRZ bit rate, it is coherent: if the NRZ bit rate does not divide evenly into the carrier frequency, the carrier is incoherent. Coherency exists when the phase shift occurs at the same point (angle) of a carrier cycle, and incoherent carriers may be phase shifted at random cycle angles which depend on the modulating NRZ bit rate (Pulse Width).

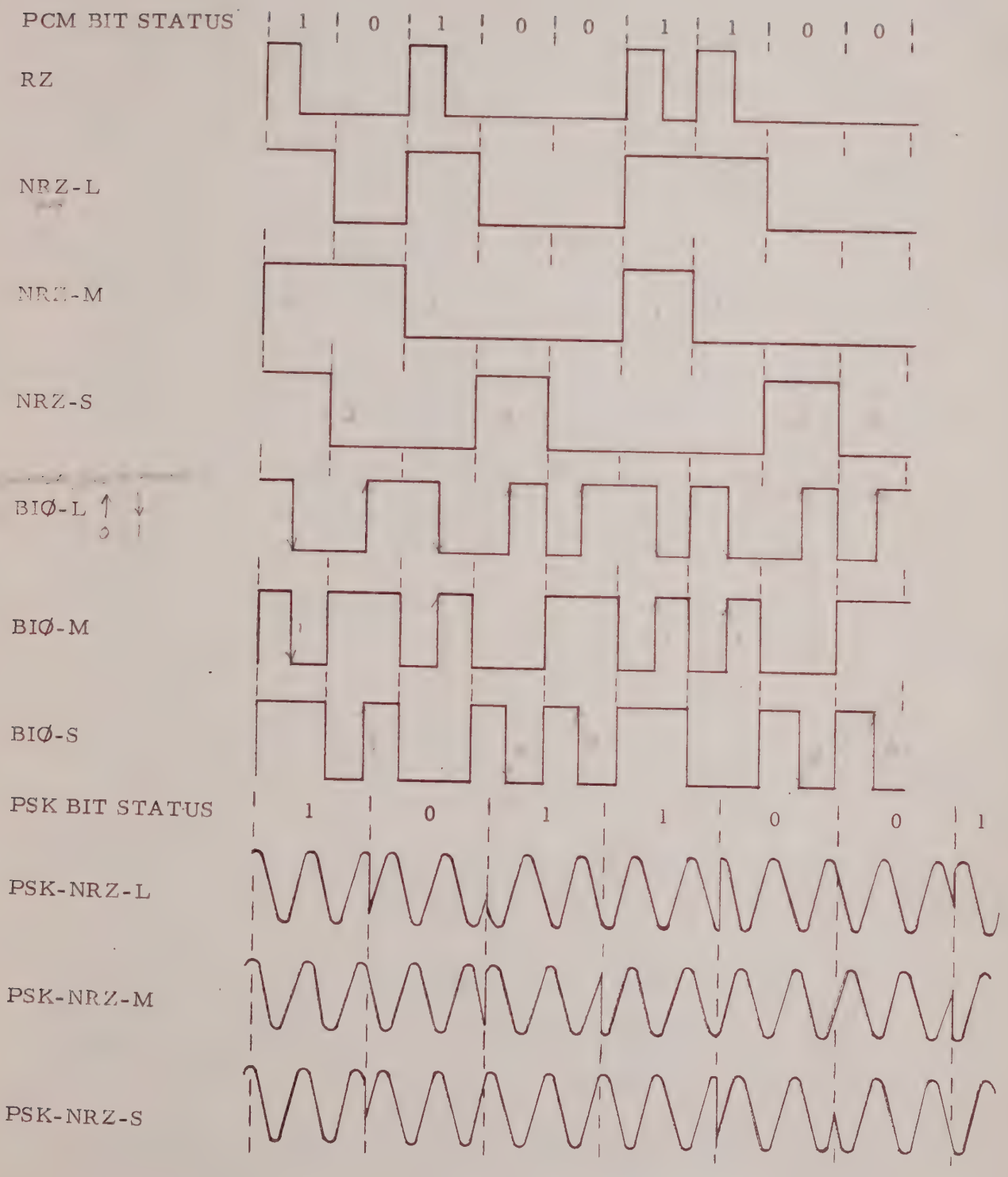


Figure 1-2. Telemetry PCM Code Format Standards

TABLE 1-2

FUNCTIONAL CIRCUIT BOARDS

Qty.	Functions	Location	Board #
2	DC Restorer-Limiter - 1/2 2fc Generator	Reference Loop Data Loop	#1000
2	VCO, DC Amp-1/2 2fc Generator-VCO Quad. Amp. Meter Amp. Ø Comparator	Reference Loop Data Loop	#1100/1700
2	Meter Circuits	Reference Loop Data Loop	#1400
1	Synchronous Detector Carrier Line Driver	Reference Loop	#1800
1	Integrator-Bit Detector	Data Loop	#1200
1	RZ Code Converter	Data Loop	#1300/1600
1	RZ to NRZ Code Converter Data and Clock Output Line Drivers	Data Loop	#1500
1	+8 volt and +12 volt DC Supply	Power Supply	#200
1	-24 volt DC Supply	Power Supply	#300
1	-4 volt, -8 volt, -12 volt DC Supply	Power Supply	#100
1	+24 volt DC Supply	Power Supply	#400

1-21. BI-PHASE PCM. Bi-Phase PCM is a phase modulated bi-level square wave and its maximum frequency is equal to the bit rate of the data; it may be considered as a special case of coherent PSK modulation.

1-22. PCM BI-LEVEL CODES. The following word definitions refer to IRIG standard formats.

a. NRZ-L.

The level of the signal is high during all "1" bit periods and returns to the low level only at the instant a "0" bit occurs. The level of the signal is low for all data "0" bits and makes a level change to high at the instant a "1" occurs.

b. NRZ-M.

The level of the signal makes a transition whenever a "1" data bit occurs.

c. NRZ-S.

The level of the signal makes a transition whenever a "0" data bit occurs.

d. RZ.

The level of the signal is high at the beginning of a "1" bit and makes a transition to low in the middle (180°) of a "1" bit. The level of the signal is low throughout a "0" bit period.

SECTION II

INSTALLATION

2-1. GENERAL.

2-2. This section describes the procedure to prepare and install the Model GPD-6. Connectors and connector designations are listed in Table 2-1.

2-3. UNPACKING AND HANDLING.

2-4. The unit is sealed in a polyethelene bag and wrapped in Kimpack insulation. All connectors are furnished with the equipment.

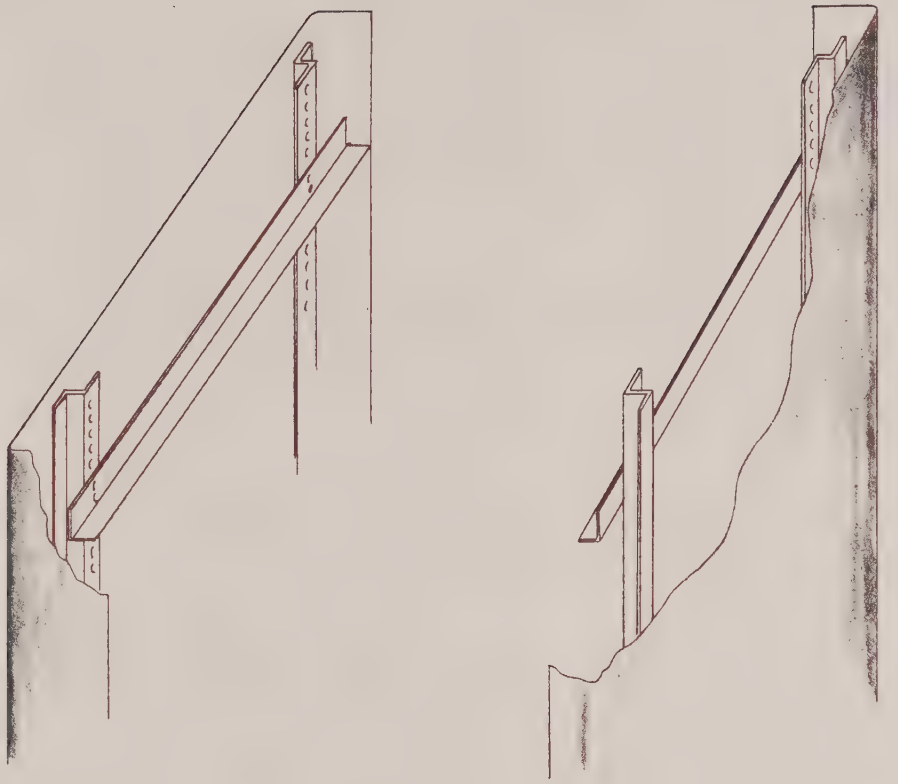
2-5. Remove the corrugated carton and protective covering, and perform a general visual inspection. Look for apparent damage to the front panel such as broken controls and indicators. Inspect the aluminum cover for scratches, dents, etc. If any damage is noticed, notify the carrier and Data-Control Systems immediately. Retain the carton and protective covering until the inspection is completed.

2-6. MOUNTING.

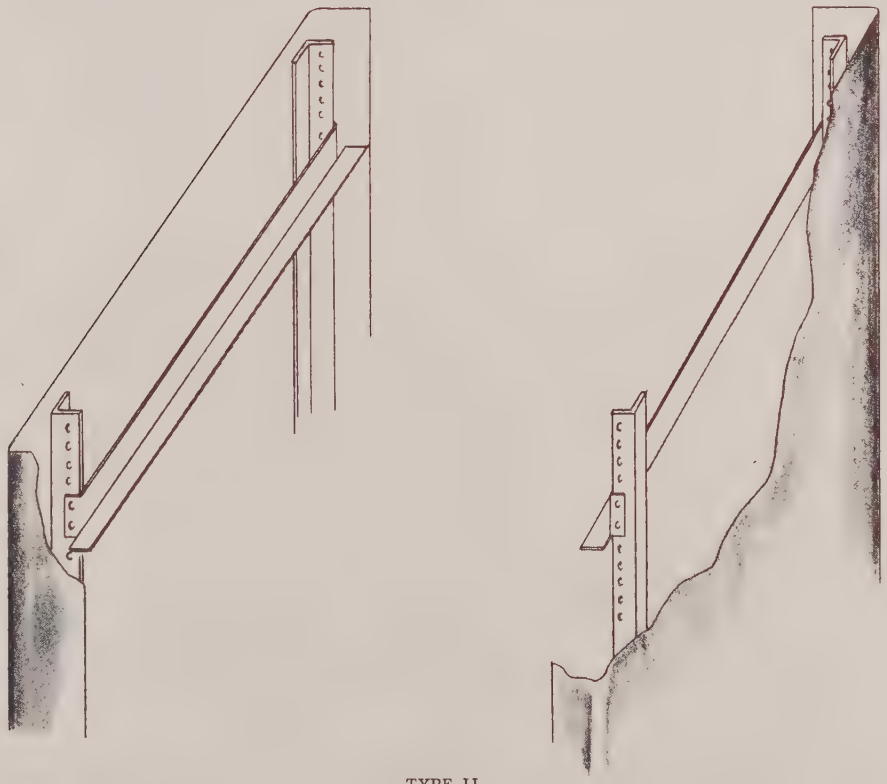
2-7. The model GPD-6 may be mounted directly in a standard 19" rack using angle brackets. The Emcor enclosure is particularly suitable since vertical angle iron supports are supplied. On each side of the enclosure an aluminum angle support is mounted horizontally, parallel to the rack side panels, and fastened to the vertical angle iron supports. Two types of angle supports are available for fastening to vertical iron supports: one with an ear, one without (see Figure 2-1.)

2-8. The housing slides in the front of the enclosure and rests upon the aluminum angles. Two tabs at the rear of the housing are fastened to the aluminum angles with screws. Four panel screws fasten the housing panel to the front of the enclosure. NOTE: Panel mounting without angle support is not recommended.

2-9. The Model GPD-6 may also be mounted on Grant slides: Micro-Slide #4425 (non-locking) 19" length, 18" travel or 20" length, 19" travel. Mounting particulars are illustrated in outline drawing DO-015272 in Section VI.



TYPE I



TYPE II

Figure 2-1. Mounting Angles, Type I and II.

2-10. CONNECTORS.

2-11. A table of main connectors is provided in Table 2-1. Individual terminals of each connector are labeled and identified on the outline drawing DO-015272.

Table 2-1. Connector Designations

CONNECTOR		MATING CONNECTOR		
Designation	Specification	Designation	Specification	Function
J801	UG-657/U	P801	UG-88C/U	Input
J802	UG-657/U	P802	UG-88C/U	CLOCK Out
J803	UG-657/U	P803	UG-88C/U	DATA Out
J804	UG-657/U	P804	UG-88C/U	PSK Carrier Out
J805	MS3102A-16S-1	P805	16S-1S	Power
J807	Burndy MS20RM	P807	Burndy PS20PM-1	(see drawing DO-015272)
J808	Amphenol 57-10360	J808	Amphenol 57-20360	(see drawing DO-015272)

2-12. COOLING.

2-13. The GPD-6 contains a muffin fan (located at the rear of the chassis) to cool the regulator power transistors. If the inlet air vent is partially or totally blocked, excessive heat may cause erratic performance or damage to unit.

2-14. If the mounting racks are air conditioned or totally enclosed be sure that the unit ambient temperature does not exceed the specified range of 0° to 40°C.

2-15. FRONT PANEL PLUG-IN MODULE INSTALLATION.

2-16. The GPD-6/TU, GPD-6/F and GPD-6/BP plug-in units are connected to the GPD-6 through Elco pins. To install a plug-in module, slide it carefully into its compartment until the Elco pins mesh with each other. Tighten the captive screw.

SECTION III

OPERATION

3-1. GENERAL.

3-2. This section contains a description of each operating control and gives instructions to operate the Model GPD-6.

3-3. OPERATING CONTROLS AND INDICATORS.

3-4. The location, function and description of each control and indicator is listed in Table 3-1. The Model GPD-6 front panel is illustrated in figure 3-1.

Table 3-1. Location and Function of Operating Controls and Indicators

Control/Switch/Indicator	Location	Function
Power Pushbutton	Control Module	Applies or disables power when depressed: lights green when power is on. Does not light if power supply short exists.
Concentric Format-Mode Switches	Control Module	Outer switch selects PSK-NRZ, Bi-Phase, NRZ or RZ input, formats: inner switch selects L, M, or S code formats of PSK-NRZ, Bi-Phase and NRZ.
Format-Mode Lights: PSK, BIØ, NRZ, RZ, L, M, S	Control Module	White lights show codes selected by Format-mode switches.
Set Pushbutton-Data Loop	Control Module	Spring-loaded pushbutton opens the Data phase lock loop and allows adjusting the Data Loop frequency on the GPS-6/F plug-in module to the incoming frequency. Lights amber when depressed.
Frequency Set Meter	Control Module	When SET pushbutton is depressed, indicates frequency difference of incoming PCM bit rate and internal oscillator.

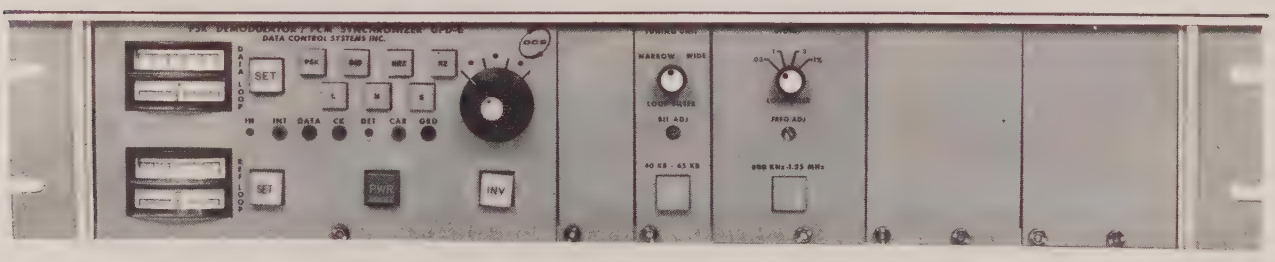


Figure 3-1. GPD-6 Controls and Indicators

Table 3-1. Location and Function of Operating Controls and Indicators (cont.)

Control/Switch/Indicator	Location	Function
Loop Stress Meter: Data Loop	Control Module	Indicates phase error of locked Data Loop.
SET Pushbutton-Reference Loop	Control Module	Spring-loaded pushbutton opens the Reference Phase Lock Loop and allows adjusting the Reference Loop frequency on the GPD-6/F plug-in module to the incoming carrier frequency. Lights amber when depressed.
Frequency Set Meter	Control Module	When SET pushbutton is depressed, indicates frequency difference of incoming PSK or BI-Ø carrier and internal oscillator.
Loop Stress Meter: Reference Loop	Control Module	Indicates loop stress of locked Reference Loop.
IN Monitor Jack	Control Module	Monitors input DATA signal.
INT. Monitor Jack	Control Module	Monitors signal at integrator capacitor.
DATA Monitor Jack	Control Module	Monitors DATA output.
CK Monitor Jack	Control Module	Monitor CLOCK output.
DET Monitor Jack	Control Module	Monitors synchronous detector output: PSK and BIØ only.
CAR Monitor Jack	Control Module	Monitors square wave output at carrier frequency. PSK and BI-Ø Formats.
GRD. Jack	Control Module	Ground reference.
INV. Pushbutton	Control Module	When depressed and lighted this pushbutton compensates for inverted input DATA.
LOOP FILTER Switch	Bit Rate Tuning Unit GPD-6/TU	Two-positions adjusts phase-Locked loop filter for NARROW or WIDE operation.

Table 3-1. Location and Function of Operating Controls and Indicators (cont.)

Control/Switch/Indicator	Location	Function
BIT ADJ. Screwdriver Control	Bit Rate Tuning Unit GPD-6/TU	Adjust Data Loop phase locked loop frequency: when Set pushbutton is depressed, adjusts VCO frequency. When DATA SET pushbutton is released, adjust loop stress to zero on Phase Meter.
LOOP FILTER Switch	Frequency Selector Unit GPD-6/F	Switch selects the loop filter bandwidth as a % of carrier frequency.
FREQ. ADJ. Screwdriver Control A	Frequency Selector Unit GPD-6/F	Adjusts Reference Loop phase lock loop frequency: when SET pushbutton is depressed adjusts VCO frequency. When reference SET pushbutton is released, adjusts loop stress to zero on Phase Meter.
OUT, X1, X3, X10 Switch	Bandpass Filter Module GPD-6/BP	Switches filter in and out of Reference Loop input, and selects gain.
NRZ-RZ Output Toggle Switch-Lower	Top Cover GPD-6	Two-position switch selects NRZ or RZ output DATA Code. RZ Out for all but "S" codes.
CLOCK Output Toggle Switch-Upper	Top Cover GPD-6	Two-position switch selects CLOCK or $\overline{\text{CLOCK}}$ for RZ or NRZ output Data.
Square Indicator Lamps	GPD-6/TU	Lit for all modes of operation: PSK, Bi-Phase, NRZ, RZ.
Square Indicator Lamps	GPD-6/F and	Lit when PSK or Bi-Ø code is selected.
Square Indicator Lamps	GPD-6/BP	Lights when PSK or BI-Ø is selected and filter is in use.

3-5. OPERATING INSTRUCTIONS.

3-6. The following instructions describe choice of tuning unit and frequency unit, the setting of the Format-Mode Switches, loop filters and selection of NRZ or RZ output DATA with appropriate output CLOCK.

3-7. CHOICE OF CORRECT BIT RATE TUNING UNIT (GPD-6/TU). The module operates in the Data Loop. Each GPD-6/TU lists the bit rate for incoming PCM-NRZ and BIØ codes: thus, type No. 9 bit rate is correct for NRZ and BIØ bit rate between 400 and 650 bps. When the incoming code is PCM-RZ, Type No. 9 is correct for RZ bit rates between 200 and 325 bps. Thus, the correct GPD-6/TU for any given bit rate will be marked with twice the incoming RZ bit rate.

3-8. CHOICE OF CORRECT FREQUENCY SELECTOR UNIT (GPD-6/F). This module operates in the Reference Loop - for PSK and Bi-Phase incoming code formats only.

3-9. For PSK carriers, simply choose the GPD-6/F Type No. that will include the carrier frequency.

3-10. For Bi-Phase carriers, the frequency of the GPD-6/F is the bit rate.

3-11. OVERALL OPERATING PROCEDURE. This procedure describes operation of the GPD-6 with PSK-NRZ, and Bi-Phase input Data Formats.

3-12. The PSK-NRZ and Bi-Phase formats require the use of the GPD-6/TU and GPD-6/F plug-in modules. The NRZ and RZ formats require use of the GPD-6/TU plug-in module. An optional GPD-6/BP plug-in module separates the PSK-NRZ carrier from a multiplex of PSK carriers.

3-13. PSK-NRZ AND BI-PHASE OPERATION PROCEDURE.

a. Insert GPD-6/TU and GPD-6/F plug-in modules into their proper front panel compartment. Tighten the captive screws.
b. Depress power pushbutton. The power pushbutton GPD-6/TU and GPD-6/F buttons will light. Allow a few minutes for the Model GPD-6 to warm up.

c. Select PSK-NRZ or Bi-Phase input code format using outer knob of Format-Mode Switch. Lights indicate format selected, and the GPD-6/TU and GPD-6/F buttons will light according to the format selected. For PSK-NRZ operation, both the PSK and NRZ buttons will light.

d. Select L, M or S input mode using inner knob of the Format-Mode Switch. Button will light indicating selection.

NOTE

Due to IRIG and DCS definitions of the Bi-Phase codes, selection of Bi-Phase-S and Bi-Phase-M must be interchanged as follows: for Bi-Phase-S, IRIG incoming format, select Bi-Phase-M on the GPD-6; for Bi-Phase-M IRIG, select Bi-Phase-S on the GPD-6. See Table 3-2. and Figure 1-3.

e. Lock Reference Loop to incoming frequency as specified in paragraph 3-14.

f. Lock Data Loop to Reference Loop output as specified in paragraph 3-15.

g. The loop filter of the GPD-6/TU and GPD-6/F modules may be adjusted to "Wide" or "Narrow" positions depending upon operating conditions.

h. Select RZ or NRZ-L data output format using lower toggle switch accessible through finger hold in top cover of the Model GPD-6. See Table 3-2.

i. To process inverted input data, depress INV pushbutton, This button will light, and DATA will be reinverted at the input to the code converter.

Table 3-2. Output Data and Clock Selection For The Various Input Formats and Modes

Input (Note 4)	NRZ-L Output Data Output Switch (Lower), Forward	RZ Output (Note 3) Data Output Switch (Lower), Rearward
Input Format Mode	Clock Output Switch (Upper)	Clock Output Switch (Upper)
NRZ-L	Rearward	Forward
NRZ-M (3)	Forward	Rearward
NRZ-S (3)	Forward	Rearward
RZ	Forward	Rearward
BIØ-L	Rearward	Forward
BIØ-M (3)	Forward	Rearward
BIØ-S (3)	Forward	Rearward
PSK		
NRZ-L	Ambiguous Polarity of Data	
NRZ-M (3)	Forward	Rearward
NRZ-S (3)	Forward	Rearward

Table 3-2. (Continued)

NOTES:

(1) Output Data Format (NRZ-L or RZ) and Output Data Clock or Clock selector switches are accessible through a fingerhold in top of the unit.

(2) The upper switch selects Clock or $\overline{\text{Clock}}$ output while the lower switch selects NRZ-L or RZ data output.

(3) RZ output of the S Modes is the complement of the true data.

(4) See Figure 1-3 for Telemetry PCM Code Format standards.

3-14. LOCKING REFERENCE LOOP TO INCOMING FREQUENCY. Two methods of locking the Reference Loop phase-locked loop to incoming frequency can be used: the first method presupposes that the incoming frequency is known; in the second method the incoming frequency is somewhere within the range of the GPD-6/F module selected. Both Reference Loop meters are used to make the adjustments: The top meter, marked "0" to "10", is used in conjunction with the REF SET pushbutton and GPD-6/F screwdriver pot, and the lower meter, marked "+" to "-", is used with the GPD-6F screwdriver pot.

Method #1 Procedure: (Incoming Frequency known)

a. Monitor PSK carrier or Bi-Phase frequency on CARrier jack using frequency counter.

b. Preset Reference Loop to incoming frequency as follows:

1. Depress and hold SET pushbutton of reference loop.
2. Set CARrier jack frequency to known or anticipated incoming frequency with GPD-6/F screwdriver pot. As the incoming and internal frequencies approach synchronization, the upper meter will swing upwards toward "10". At an exact zero beat, the meter may suddenly drop back to "0". (This is readily observable at frequencies below 20kHz).
3. Release the SET pushbutton. The reference loop is now locked to the incoming frequency, and the meter will return to "0".

c. To adjust for any slight loop stress that may remain, observe the lower (+ to -) meter for slight + or - deviation. Adjust GPD-6/F screwdriver pot until this meter is centered on "0".

Method #2 Procedure: (Carrier Frequency undetermined)

a. Adjust Reference Loop to incoming frequency as follows:

1. Depress and hold REF SET pushbutton.

2. Slowly adjust GPD-6/F screwdriver pot observing upper (0 - 10) meter. Several peaks of various levels may be found, depending on operating conditions, such as the nature of the incoming Data and the amount of noise present. Select the peak producing the greatest meter deflection towards "10": then release the SET pushbutton. With "clean" Data the meter indicator should return to "0". If there is still a substantial meter deflection, the wrong peak may have been chosen or noise may be present. Repeat steps (1) and (2) until the correct peak has been found.

NOTE

Large amounts of noise can cause residual meter indications even at the correct peak.

b. To adjust for any slight remaining loop stress observe the lower (+ to -) meter for slight + or - deviations. Adjust GPD-6/F screwdriver pot until the meter is centered on "0".

3-15. LOCKING THE DATA LOOP TO REFERENCE LOOP OUTPUT. When operating on PSK and Bi-Phase code formats, the Data Loop must be locked to the Reference Loop output. The locking procedures are the same as Methods #1 and #2 of paragraph 3-14.

Method #1 (Incoming Bit-Rate known)

a. Lock Data Loop of Reference Loop output following the procedure of Method #1 in paragraph 3-14. Use GPD-6/TU screwdriver pot, Data Loop meters and DATA SET pushbutton. Monitor bit-rate at CK jack with frequency counter.

Method #2 (Incoming bit-rate undetermined)

a. Lock Data Loop to Reference Loop output by following the procedure of Method #2 in paragraph 3-14. Use GPD-6/TU screwdriver pot, Data Loop meters and DATA SET pushbutton.

3-16. PCM-NRZ AND PCM-RZ OPERATION PROCEDURE.

3-17. If the incoming DATA is NRZ or RZ the Reference Loop is not used, and only the Data Loop is set up as described above in paragraphs 3-13 and 3-15. To lock the Data Loop to incoming DATA, the GPD-6/TU is adjusted to the incoming DATA and not to the output of the Reference Loop.

3-19. When the Mode Switch is in the "L" position and the DATA output toggle switch is in the "NRZ-L" position, all GPD-6 code converters are bypassed.

Example: NRZ-M DATA IN will be NRZ-M DATA OUT.

3-20. USE OF OUTPUT DATA AND CLOCK OUTPUT TOGGLE SWITCHES.

3-21. Table 3-2 lists the uses of RZ-NRZ and CLOCK-$\overline{\text{CLOCK}}$ toggle switches. See Notes 3 and 4.

SECTION IV

THEORY OF OPERATION

4-1. GENERAL.

4-2. This section presents an overall functional description of the GPD-6. The description covers overall code format selection, the two major loops, signal routing, and processing. In addition, a detailed functional description is provided which gives an analysis of each functional block on the simplified block diagram (figure 4-1). The detailed functional description describes the schematic diagrams in Section VI and special drawings accompanying the discussions.

4-3. OVERALL FUNCTIONAL DESCRIPTION.

4-4. The Model GPD-6 consists of two phase-locked loops (reference loop and data loop), two Code Converters, (RZ and NRZ), Plug-in units GPD-6/TU, GPD-6/F optional GPD-6/BP and five dc power supplies (±24, ±12, ±8, -4V dc). The reference loop demodulates the incoming PSK carriers and Bi-Phase coded signals; the PSK carrier is demodulated and the modulating PCM-NRZ code format is removed from the carrier; the Bi-Phase signal is converted to NRZ-L. The data loop detects and reconstructs PCM code data bits and produces an in-phase, coherent output clock to match the PCM code format. The input PCM code format signal to the data loop can also be raw incoming signals taken from recorders or receivers. Input code format routing and conversion is selected by the front panel concentric Mode/Format switch which determines the type of operation required to process the input code format. The output data and clock signals may be either RZ format or NRZ-L by direct selection at the front panel format mode switch. Details of input/output code format selection are contained in Section III. The separate functions of the Reference Loop and Data Loop are shown in Figure 4-1. Each loop contains a DC Restorer, Limiter, Doubler and Phase-Locked Loop; since these circuits are identical for each loop, they are described only once in the detailed functional description.

4-5. REFERENCE LOOP (PHASE DEMODULATION).

4-6. The Reference Loop accepts and demodulates PSK carriers and PCM Bi-Phase signals to derive the PCM-NRZ code family bits which modulate the PSK carriers and Bi-phase signals. The Reference Loop extracts NRZ-L, NRZ-S

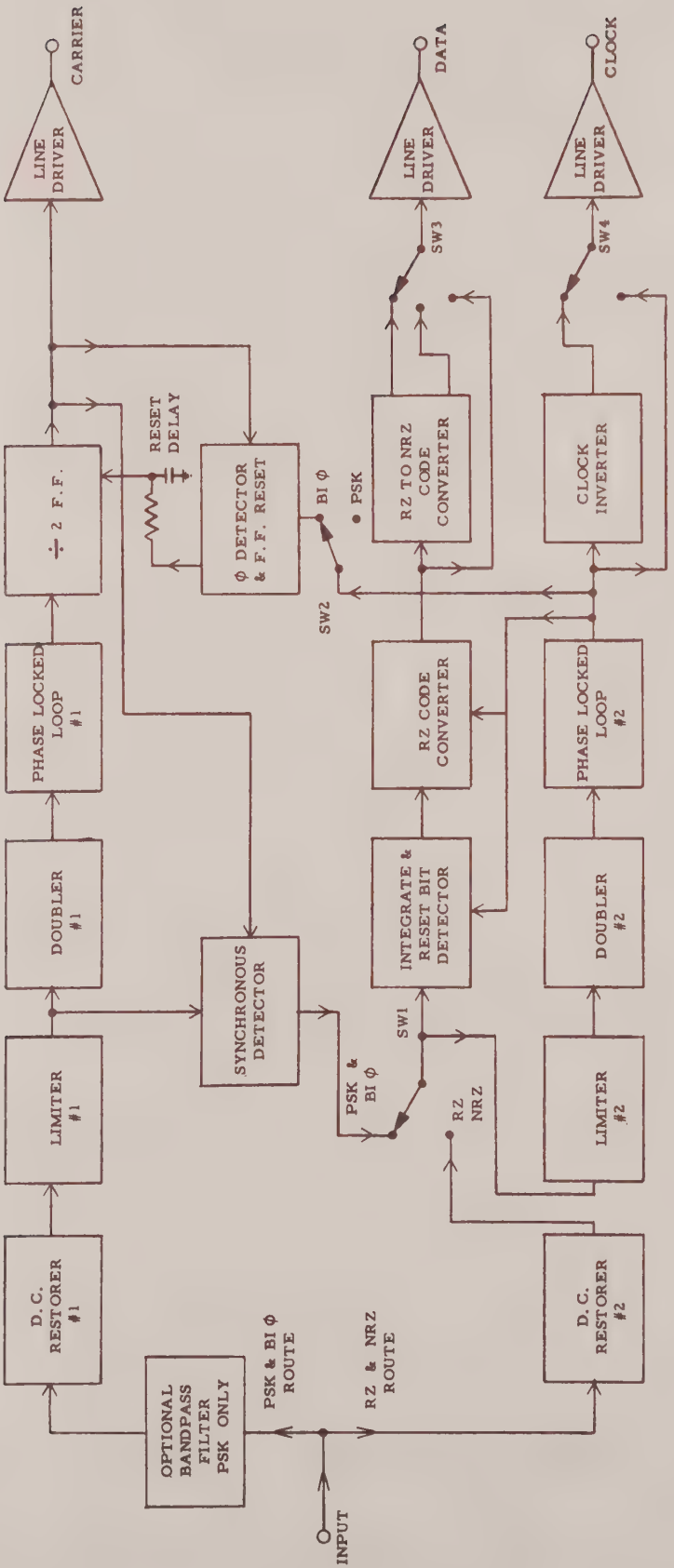


Figure 4-1. GPD-6 Simplified Block Diagram.

or NRZ-M bits from the PSK carriers, and NRZ-L from the Bi-Phase signals. These PCM bits are then detected and reconstructed in the Data Loop. As shown in figure 4-1, the Reference Loop contains a dc restorer, limiter, doubler, phase-locked loop, and a synchronous detector.

4-7. A front panel plug-in frequency unit (GPD-6/F) supplies the reactive and tuning components for the loop. An optional plug-in unit (GPD-6/BP) separates a particular PSK carrier from a multiplex of PSK carriers.

4-8. PSK DEMODULATION. PSK carriers are phase-modulated by NRZ data bit level transitions. A coherent PSK carrier contains an integral multiple of cycles per NRZ bit rate, and an incoherent PSK carrier contains fractional multiples of cycles per NRZ bit rate. Either code carrier can be demodulated by the PSK phase-locked loop and synchronous detector. A dc restorer corrects base line fluctuations before carrier limiting. The limiter reshapes the carrier into a square wave which is then fed to a doubler to generate two square wave pulses for each limited square pulse. The phase comparator detects the phase of the doubled carrier with respect to a timing signal generated in the VCO and produces an error voltage which locks the VCO signal to the doubled carrier. The VCO frequency is determined by the GPD-6/F frequency plug-in unit. The VCO frequency (divided by 2) and the limited carrier square wave are fed to a synchronous detector for phase demodulation. In the synchronous detector, phase changes are transformed into level changes. The resultant is raw PCM, NRZ family data bits to be processed and reconstructed in the Data Loop.

4-9. BI-PHASE DEMODULATION. The Bi-Ø signal is a special case of PSK where the PSK carrier is coherently phase modulated by a PCM signal whose bit rate is equal to the carrier frequency. Detection of Bi-Ø-M, Bi-Ø-S, and Bi-Ø-L is accomplished as is the PSK in the Reference Loop. The output of the synchronous detector is NRZ-M, NRZ-S, and NRZ-L or $\overline{\text{NRZ-L}}$ respectively. This signal is routed to the data loop and is locked on by the data phase-locked loop.

4-10. The demodulation of the Bi-Ø-L in the reference loop results in ambiguous NRZ-L or $\overline{\text{NRZ-L}}$ being fed to the data loop. After the data loop has locked to this ambiguous signal, the ambiguity can be resolved. This is done by a phase comparator/reset circuit that compares the $\frac{\text{VCO}}{2}$ supplied to the synchronous detector in the reference loop to the clock in the data loop. If the phase relationship is incorrect, the $\frac{\text{VCO}}{2}$ to the synchronous detector is changed in phase, thus changing the synchronous detector output from $\overline{\text{NRZ-L}}$ to NRZ-L.

4-11. DATA LOOP (PCM BIT DETECTION).

4-12. The Data Loop accepts, detects, and reconstructs raw PCM-NRZ and PCM-RZ data signals. The loop contains a dc restorer, limiter, doubler, phase-locked loop, integrator and bit detector. A front panel plug-in unit (GPD-6/TU) supplies the reactive and tuning components for the loop.

4-13. Non-Carrier PCM-NRZ or RZ data is fed first to a DC restorer; Reference Loop NRZ data is switched directly into the Data Loop integrator. The Data Loop performs two synchronous operations on the NRZ or RZ data; an internal timing signal is generated by locking on the input data frequency, a clean data signal is generated by integrating the input signal at times governed by the internal timing pulses, and the integrated waveform is detected to establish reconstructed output data. The internal timing signals (VCO and $\overline{\text{VCO}}$) are generated by a phase-lock-loop consisting of a data doubler, voltage controlled oscillator, phase comparator, loop filter and dc amplifier. The output clock is derived from the VCO and $\overline{\text{VCO}}$ signals in the Code Converters. The input data is analyzed in the Integrator, which makes decisions based on the average power contained in the "1" and "0" data bits. Since the integrator is timed by the phase-coherent VCO signal, integrations occur at the exact incoming data bit rate. Integrations are performed on the minimum pulse width of all code formats, therefore the VCO must run at twice the incoming NRZ and MNRZ bit rates, and at four times the incoming RZ bit rate. The positive ("1") or negative ("0") integrating operate a bit detector current switch and flip-flop which together generate a reconstructed data pulse train. This reconstructed data fed into the Code Converter. The Bit Detector output data may be converted to an equivalent NRZ-L or RZ format in the Code Converter. All input Code Mode and Format Selections are controlled by a front panel switch. Selection of output code is accomplished with internal switches readily accessible through a hole in the top cover.

4-14. The reconstructed data output from the bit detector is NRZ-L, NRZ-M, NRZ-S or RZ depending on the input format selected. An input format of NRZ-L (or the result of detecting Bi-Phase-L in the Reference Loop) by-passes the RZ and NRZ-L code converters, and is fed directly to the line drivers. All other input code formats are converted to either RZ (in the RZ code converter) or NRZ-L (through both the RZ and NRZ-L code converters). The coherent output clock is derived in the code converters from the VCO signal of the data loop VCO.

4-15. DETAILED FUNCTIONAL DESCRIPTION.

4-16. The following paragraphs analyze each functional block shown for the reference and data loops on the simplified block diagram (figure 4-1). The descriptions refer to the schematic drawings contained in Section VI and special illustrations accompanying each discussion. The following blocks are discussed: dc restorer, limiter, phase-locked-loops (same for Reference and Data Loops), ÷2 FF and Bi-Phase Detector, synchronous detector, integrator, bit detector, RZ and NRZ Code Converters, meter circuits, line drivers, power supplies.

4-17. Component reference designations on individual schematics are abbreviated and are referenced in the discussion without their first significant number, which designate the printed circuit board. For example: "C1002" is designated "C2" in the text and is situated on circuit board "1000".

4-18. DC RESTORER (See drawing GW-015532). Input data signals to either reference or data loops first go through a dc restorer circuit to remove base line fluctuations. The input signal, with dc or low-frequency ac on it, is ac coupled out of emitter follower Q2 with dc restorer capacitors C2 and C3. CR3 clamps the negative side of the signal through C2 to ground. CR4 clamps the routine side of the signal through C3 to ground. These two wave forms are summed by resistors R4 and R5. The result is a waveform which is centered about ground. The base current of emitter follower Q3 is compensated for by limiter centering potentiometer R16.

4-19. LIMITER (See drawing GW-015532). The limiter standardizes incoming signals of varying amplitudes to a square wave of approximately 1.2V peak-to-peak. Positive-going signals at Q4 emitter disconnect CR5 from the junction of R27 and CR6, allowing R26 and R27 (through CR6 and R31) to turn-off Q5. Negative-going signals at Q4 emitter cause CR5 to conduct, thus pulling down the junction of R27 and CR6, disconnecting CR6 from the junction of R28 and R30, allowing R28 and R29 to turn-on Q5. Q5 and Q6 form a differential pair of current switch. As the base of Q6 is grounded, a signal swinging around ground applied to the base of Q5 will either cause all the current from the emitter resistors R32 and R33 to flow through Q5 or none. When none flows through Q5, all of it must go through Q6. This current flowing from the collector of Q6 pulls the junction of CR7 and CR8 upward until caught by CR7 at approximately 0.6V above -12V. When collector current does not flow, R38 pulls the junction of CR7 and CR8 down until it is caught by CR8 at a point 0.6V below -12. Output of the limiter at test point T1002 and into the doubler is therefore -12V ±0.6.

4-20. DOUBLER (See drawings GW-015532 and TW-015280). This function consists of two circuits connected by a doubler capacitor in the plug-in unit (GPD-6/TU, GPD-6/F). The doubler generates two square pulses for every input data square pulse; that is, the doubler generates a pulse for every input signal level change. The doubled data signal is compared in the phase comparator with the equivalent frequency VCO timing signals (see drawing GW-015532).

4-21. The first part of the doubler circuit is mounted on the dc restorer-limiter board. When Q8 is turned on by the -11.4V signal from limiter, Q10 is turned off because its base is clamped to -12.0V. The current flowing in the collector of Q8 pulls the base of Q9 to 0.6V below +12V or +11.4V (determined by CR9). Q9 is turned on and delivers a constant current determined by the +24V supply, the base voltage, and R45. This constant current is derived from a capacitor (in the GPD-6/TU, or GPD-6/F) whose other terminal is tied to the emitter of a grounded -base stage (low impedance). This capacitor is charged linearly until held by CR12 at +5.6V. This 5.6V is held while CR12 continues to supply the current to Q9 as long as the input from the limiter remains plus. When the input to Q8 is turned off, R43 pulls the base of Q9 positive until caught by CR10 at +12.6V. The emitter tries to follow the base upward until caught by CR11 at +12.6V. The emitter tries to follow the base upward until caught by CR11 at +12.6V. Q9 is therefore turned off and collector current ceases to flow. Simultaneously, Q10, whose base is clamped at -12.0V, is turned on and a constant collector current flows determined by the emitter resistor R44, the -24V supply, and the base voltage of -12V. This constant collector current is supplied to the capacitor that has just been charged to +5.6V by Q9. This capacitor is now discharged until the collector of Q10 is caught by CR13 at approximately -0.16V. CR13 will continue to supply the current to Q10 for the rest of the negative-going period of the limiter output. The charging and discharging currents are equal and are chosen, along with the capacitor value, to give charge and discharge times that are equal to one-half of the minimum data pulse width. Q7 base is connected to the frequency control bus whose dc voltage changes in accordance with changes of frequency in the phase-locked loop. This voltage causes Q7 to draw less current from Q9 and Q10 as the incoming frequency increases, permitting Q9 and Q10 to supply more current to the capacitor as the data pulse becomes narrower, thereby maintaining charge and discharge times equal to one-half the data period regardless of data frequency changes.

4-22. The second half of the doubler is on the phase comparator board and is coupled to the first by the aforementioned capacitor in the plug-in. This capacitor is tied to the emitter of grounded-base stage Q1. The bias of Q1 is such that its quiescent collector voltage is +12.8V. The resulting slight conduction of CR8 is compensated for by R16, causing the bases of both Q2 and Q3 to be at ±12V.

4-23. As an example, suppose that the capacitor is charged to +5.6 volts as previously described. While it is being charged, the emitter of Q1 is pulled up causing its collector to rise also; CR8 conducts, pulling the base of Q3 positive, turning Q3 off and Q2 on. The collector Q3 goes minus and the collector of Q2 plus. When the voltage on the capacitor approaches the +5.6 volt value, no more current is drawn from the capacitor; the emitter of Q1 drops, and its collector drops back to its nominal +12.8 volts. This allows the bases of Q2 and Q3 to assume their balanced condition. This condition continues as long as no current is being put in or taken out of the capacitor. If the input signal is now reversed, the capacitor discharges toward -0.6 volts. This drives the emitter of Q1 down, causing its collector to decrease. CR7 now conducts, pulling the base of Q2 down and causing Q2 to turn on and Q3 to turn off. Again, the collector of Q2 goes plus and the collector of Q3 goes minus, but only for the duration of the discharge time. The collectors of Q2 and Q3 generate plus and minus pulses respectively each time the input data changes polarity. Because of the capacitor and current values chosen, the pulse width is one-half the data pulse width. One output pulse of one-half data pulse width is generated when the input goes plus and another similar pulse when the input goes minus, effectively creating a doubled frequency. Q6 and Q7 are tied in parallel with Q2 and Q3 and are used to supply isolated quadrature signals to the the doubler test point and the meter circuit. Q5 is used in a "lockout" circuit that disables the doubler circuit when an external pin is grounded.

4-24. PHASE-LOCK-LOOP. This loop (figure 4-2) consists of a data doubler, phase comparator, loop filter, dc amplifier and VCO. The VCO operates at a nominal rate selected by the tuning unit in use, and a VCO quadrature signal is compared with the output signal of the doubler in the Phase Comparator. Since the doubler frequency is derived from data, any change in the data frequency with respect to the VCO frequency produces a net voltage in the phase comparator. This net voltage is fed back to the VCO through the loop filter and dc amplifier to bring the VCO frequency back in correspondence with the data frequency. When the VCO remains in correspondence with data, the loop is "locked". The "locked" VCO generates the VCO and $\overline{\text{VCO}}$ signals to control integration, bit

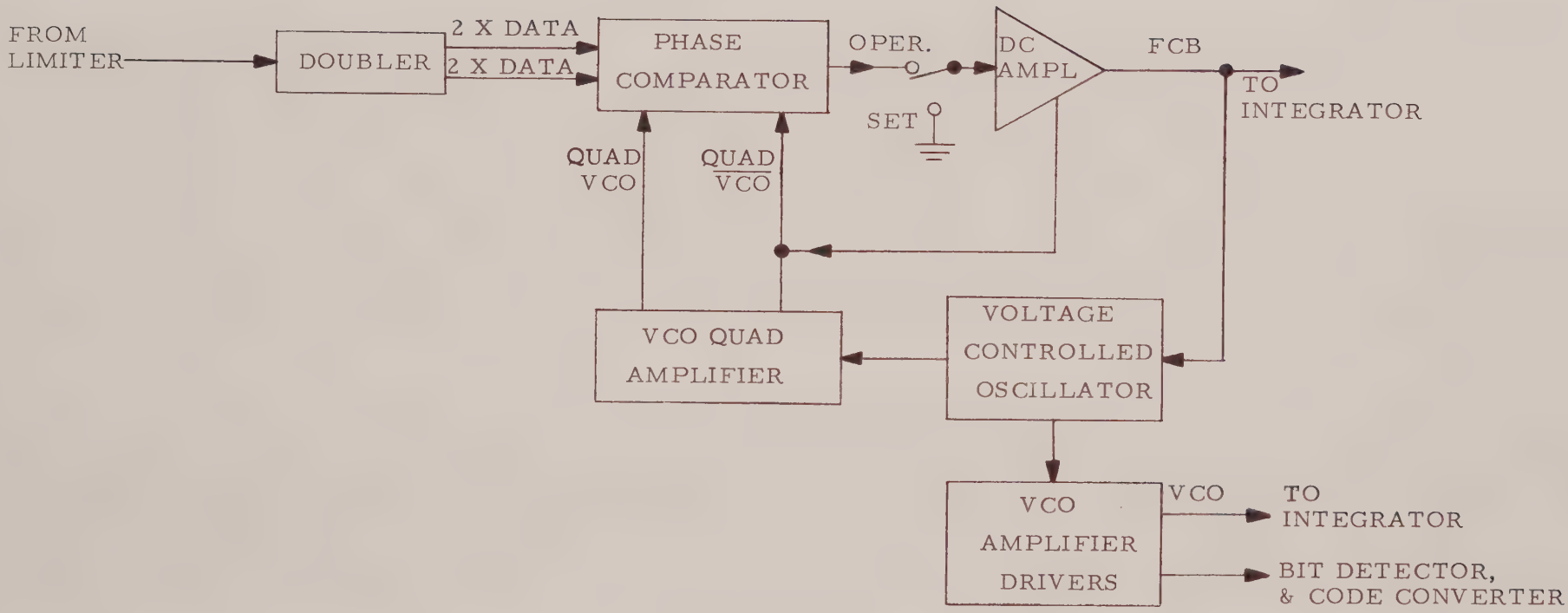
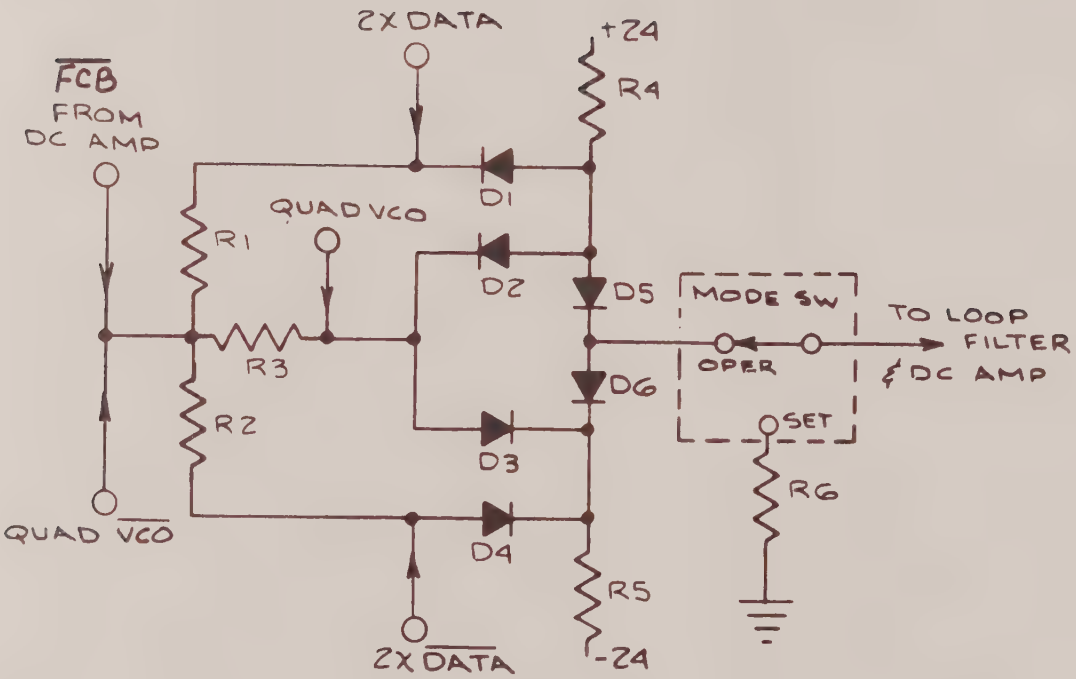


Figure 4-2. Phase-Locked-Loop.

detection, and the timing of the code converter. A clock signal is subsequently produced by the code converter in synchronization with data for any of the code formats.

4-25. PHASE COMPARATOR. The Phase Comparator (figure 4-3) compares two quadrature VCO signals with the 2X data doubler outputs. When these two signals are in quadrature (same frequency), the average output of the phase comparator is zero. The Phase Comparator consists of two AND gates D1-D2 and D3-D4, and OR gate D5-D6. The junction of D5-D6 is at 0 volts whenever both AND gates are disabled. When either AND gate closes, D5 or D6 will be reversed biased so that their common junction will go either positive or negative. When 2X data and quad VCO are both negative, D5 is reversed biased due to AND gate D1-D2 closing, and a negative voltage appears at the output junction. When quad VCO and 2X data are both positive, D6 is reversed-biased to produce a positive voltage at this junction. The resultant uniform output waveshape averages zero in the loop filter. When the two input signal pairs change phase by slipping with respect to each other, the output waveshape becomes non-uniform with net positive or negative pulses, depending upon the direction of the phase change. These non-uniform pulses are averaged in the loop filter to produce a net positive or negative voltage which controls the VCO frequency in a direction to cancel the original phase difference. The loop filter output feeds the high impedance dc amplifier.

4-26. VOLTAGE CONTROLLED OSCILLATOR. The Voltage Controlled Oscillator (VCO) generates a triangular wave which is converted to two square waves to time all internal operations of the Model GPD-6: integration, bit detection, synchronous PSK and Bi-Ø detection ambiguity resolution, and input code format conversion. In addition to the VCO and $\overline{\text{VCO}}$ timing signals, a quadrature amplifier/generator produces timing signals 90° out of phase with the VCO and $\overline{\text{VCO}}$ signals; these phase-shifted timing signals are compared in the phase comparator with the 2 X data signal from the doubler. The VCO or $\overline{\text{VCO}}$ internal signal is converted to the output clock or $\overline{\text{clock}}$ in the code converters. The timing capacitor and bit rate adjustment potentiometer in the GPD-6/TU determine the nominal frequency of the VCO; feedback from the DC Amplifier (frequency control bus, F. C. B.) locks the VCO frequency to correspond with the incoming data bit rate and phase.



PHASE COMPARATOR

Figure 4-3. Phase Comparator Circuit

4-27. The following discussion describes drawing TW-015284. A triangular voltage wave is generated across the timing capacitor by linearly charging and discharging the capacitor through Q3 and Q4 respectively. The emitter-coupled pair, Q2 and Q3, is a current switch consisting of CR1, CR2 and CR5-CR8. The tunnel diodes provide a voltage toggle switch since their junction is switched alternately from the low voltage state to the high voltage state and vice-versa by diodes CR5 and CR6. Zener diodes CR5 and CR6 provide switching voltages to bias CR5 and CR6 alternately on and off; emitter follower Q6 transmits the timing capacitor voltage to the zener diodes. The alternate conduction of these two diodes, switches the tunnel diode junction to operate current switch Q2-Q3. The total action of the diode toggle switch is to operate the charging and discharging of the timing capacitor. When Q3 turns off, Q2 turns on biasing Q4 on and discharging the timing capacitor. When Q3 turns on, Q2 turns off biasing Q4 off and charging the capacitor.

4-28. Note that the VCO timing capacitor is tied to the low impedance emitter of the grounded stage base, Q5. This means that the timing capacitor alternately pulls and pushes the emitter when it is charged and discharged, causing the collector to swing plus and minus around ground. The collector of Q5 is connected to the integrator and bit detector board where VCO and $\overline{\text{VCO}}$ drivers are located. When Q5 is turned off, its collector is pulled negative by R28 and R29 until caught at -0.6 Volts by the base of Q15. Its positive swing is caught at +0.6 Volts by diode CR19. When Q15 is turned on, Elco terminal 15, labeled "J1200-15" is pulled to -0.6 Volts through saturated Q15 and diode CR20. When Q15 is turned off, Q16 is turned on by R30 and the Elco terminal is pulled to -4 Volts by the saturated Q16. This point is therefore very low impedance and is used to drive the code converters, bit detector etc. One more inversion thru a similar circuit generates a low impedance $\overline{\text{VCO}}$ signal.

4-29. PHASE ERROR OR LOOP STRESS METER. The function of this meter is discussed in the DC AMPLIFIER/LOOP FILTER section.

4-30. In addition to the Frequency Adjust potentiometer, the frequency range and symmetry of the VCO may be adjusted with R5 and R15 respectively. The Frequency Range potentiometer regulates the current flowing through the emitter-coupled current switch Q2-Q3. The VCO symmetry potentiometer regulates Q4 emitter current to control the discharge current of the timing capacitor; this adjustment assures that charge and discharge times are equal.

4-31. VCO QUADRATURE AMPLIFIER.

4-32. Located on the Phase Comparator board (see drawing TW-015280), this circuit converts the triangular wave from the VCO to a square wave in quadrature with the VCO and $\overline{\text{VCO}}$ signals.

4-33. The VCO quadrature amplifier consists of the current switching pair Q10 and Q11 biased to switch at the midpoint of the triangular wave form. C5 is an emitter coupling capacitor to eliminate degeneration by R34, R35, and R36 the current setting resistors and balancing potentiometer. The Q11 base is pegged to +8.8V, the nominal center of the triangular wave from the VCO applied to the base of Q10. When the Q10 base goes negative, its emitter follows, and through C5 pulls the emitter of Q11 below its base turning off Q11. When the base of Q10 goes positive, Q10 is turned off because its emitter is tied to the emitter of Q11 by C5. Current is thus switched between R30 and R31 at the midpoint of the rise and fall of the triangular waveform applied to the base of Q10. The resulting square wave is therefore in quadrature with the previously derived square wave that was applied to the VCO drivers. This new quadrature VCO wave is taken from R31 and applied to the phase comparator. R30 and C7 are used to supply a small amount of high frequency compensation.

4-34. LOOP FILTER-DC AMPLIFIER. The Loop Filter integrates the pulses from the phase comparator to supply the dc that will control the VCO. The R and C components for the two-position filters are in the GPD-6/TU and GPD-6/F plug-ins. Any dc voltage that may appear on the filter is applied to the high input impedance emitter follower Q11. The emitter of Q11 will always be below its base, 0.6 volts. This is compensated for by CR13 and R44, the junction of which will very nearly match the base of Q11.

4-35. Q10, Q9, Q8 and Q7 constitute a nearly unity gain amplifier with three inputs and two outputs. The three inputs are: the base of Q10 from the loop filter; the base of Q7 from the frequency adjust potentiometer in the tuning unit; and the junction of R37 and R38 from the FCB zero-set potentiometer. The non-inverted outputs are the FCB at the junction of CR9 and R31, the voltage which controls the VCO, and the second is the emitter of Q8 labeled $\overline{\text{FCB}}$. The $\overline{\text{FCB}}$ is connected back to the phase comparator gates to prevent the voltage appearing on the filter from closing the gates. First consider a negative voltage applied to the base of Q10. This causes the base of Q9 to go plus and the collector of Q9 to go minus, because it is supplied by two current sources, Q8 and Q7. As the

collector of Q9 and the top of R32 go minus, so must the lower end of R32 and the base of Q8 go minus because they are tied to the current source Q7. The emitter of Q8 follows its base down until the current fed back from the emitter of Q8 to the emitter Q10 through R37 equals what it was initially because R32 has the same voltage drop across it as it had initially and because the emitters of Q8 to Q10 have the same voltage relation, the output taken from the collectors of Q8 and Q9 must follow the downward swing of Q10 which, of course, follows the minus voltage applied to its base. CR11 provides an offset between the emitters of Q8 and Q10 so that, with adjustment of the FCB zero potentiometer, R39, the second output from the emitter of Q8 may be set to exactly the voltage appearing on the base of Q10. This output is in phase with and always tracks the input.

4-36. The third input to the amplifier is the base of Q7. Its input from the frequency adjust potentiometer in the tuning unit must change the output of the amplifier going to the VCO but must not change the voltage being fed back to the phase comparator. When the frequency adjust potentiometer is counted, approximately two milliamps, will be supplied to R32. If the voltage on the base of Q8 is less than enough to turn it on, Q10 will be turned on harder which will turn on Q9. Q9, in parallel with R34, will pull the top of R32 up until the two mills from Q7 is taken care of plus enough base current from Q8 to turn it on. Q8 turns on enough to reduce the current through Q10 and the base drive of Q9. The current from Q9 plus the current from R34 will now just balance current from Q7 and the base current being negligible, the voltage drop across R32 is determined by the current from Q7. Changing this current will change the voltage drop and hence the voltage at the top of R32, the bottom being effectively pegged by the base of Q8. Note that the output voltage at the collector of Q8 can now be changed by the tuning unit potentiometer without changing the voltage being fed back to the phase comparator, and without the voltage to the base of Q11 changing.

4-37. In practice it is desirable to match the open-loop VCO frequency to the DATA frequency. Under these conditions, the output from the phase comparator, when locked, will be nearly zero. This is indicated by the Ø Meter which is connected to the $\overline{\text{FCB}}$ bus. In the event that the frequencies do not quite match, the phase comparator will develop a voltage which, when added to the preset voltage will match the local VCO in frequency and phase to the doubled DATA frequency. This voltage actuates the Ø Meter (also known as loop stress) indicating the direction and amount of mismatch so that a correction may be made with the tuning unit potentiometer without opening the loop. The output of the amplifier at

the collectors of Q9 and Q8 is nominal 6 volts above ground and is dropped back to operate around ground by the zener CR10 and resistor R31. The emitter follower Q1, provides low impedance for the dc voltage to operate the VCO.

4-38. DIVIDE BY TWO FLIP-FLOP (Reference Loop). The Reference Loop VCO (see drawing RW-015283) triggers flip-flop Q3-Q4 on each positive pulse; therefore, the output of the flip-flop is the reference loop $\frac{VCO}{2}$. An auxiliary trigger input C14 and C18 is normally disabled, but becomes active for the Bi-phase-L code when enabled by the phase comparator reset analog circuit.

4-39. BI-PHASE DETECTOR/RESET (Reference Loop). This circuit (figure 4-4) is the Bi-phase-L code ambiguity resolver. It compares the phase relation of the Data Loop VCO and the Reference Loop $VCO/_2$. If these two timing signals are out of phase, the flip-flop output is phase shifted 180° to bring the Reference Loop $VCO/_2$ in phase with the Data Loop VCO. This phase shift is reflected to the synchronous detector where the reference loop $VCO/_2$ determines Bi-Phase-L carrier phase detection and conversion to NRZ serial data. The reset and delay circuit is illustrated in Figure 4-4 and drawing RW-015283. The Data Loop VCO and the Reference Loop $VCO/_2$ taken from the Q4 collector, operate a OR gate, CR20 and CR21. When the two VCO signals are in phase, point A alternates between 0 and -5.1 volts. After several cycles, the reset delay capacitor in the GPD-6/F tuning unit charges to -4.5 volts. This negative voltage keeps the auxiliary flip-flop trigger below the point where the Reference Loop VCO can trigger the flip-flop. When the two VCO signals are out of phase, point A is kept at ground, and the auxiliary trigger is enabled. For convenience, label Q3 the "reset" side and Q4 the "set" side. The set and reset triggers are enabled or disabled by their respective collector outputs and the auxiliary trigger is enabled or disabled by the condition of point B. With point B at ground, and the flip-flop set (Q4 collector at 0 volts), the next positive reference VCO tries to reset the flip-flop. However, the auxiliary trigger on the set side is also enabled; this allows the positive reference VCO pulse to be applied simultaneously to the set and reset sides. The simultaneous trigger application forces the flip-flop to remain in its previous set state, achieving 180° phase shift. The $VCO/_2$,

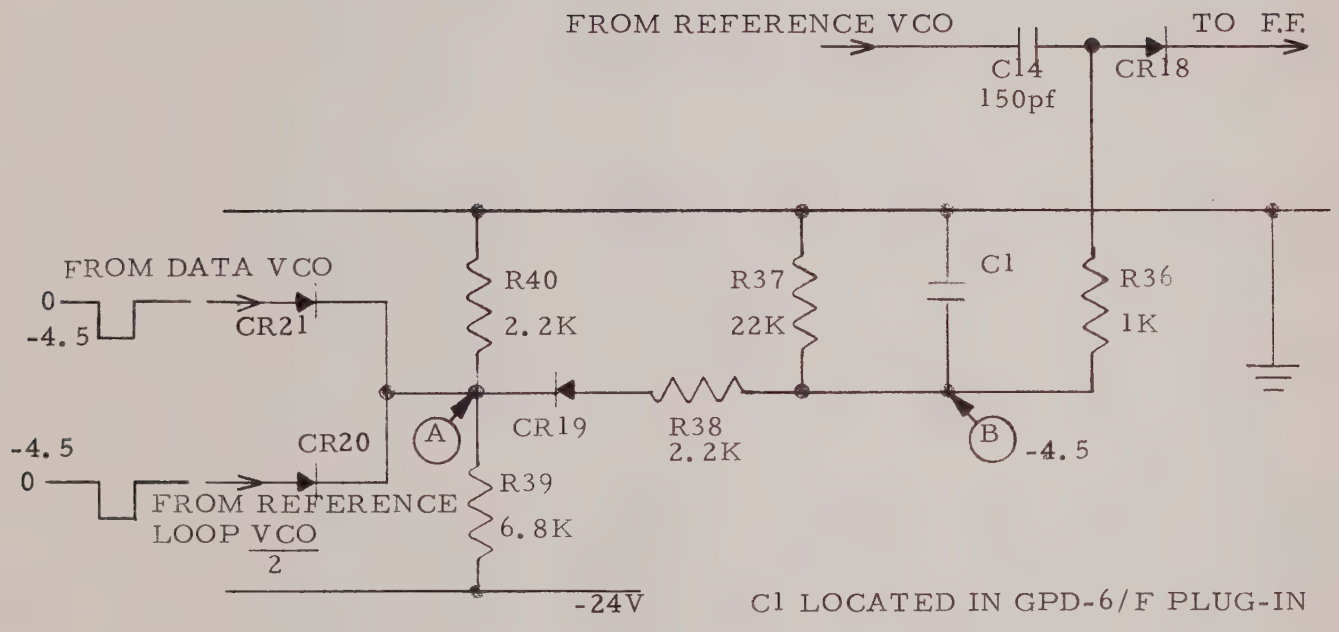


Figure 4-4. BIØ-L Bit Detector/Reset Circuit.

shifted 180°, now is in the proper phase to yield valid NRZ data from the Bi-phase-L carrier. Also, the $VCO/_2$ and the Data Loop VCO are in proper phase and the reset delay capacitor charges to -4.5 volts to disable the auxiliary flip-flop trigger.

4-40. SYNCHRONOUS DETECTOR (Reference Loop). The synchronous detector detects phase and converts Bi-phase and PSK signals to NRZ family codes. The Bi-phase Detector/Reset circuit provides Bi-phase-L code ambiguity resolution prior to phase detection, and is inactive for all other codes.

4-41. The synchronous detector consists of two symmetrical loops which act as a switch. When the $VCO/_2$ and the Bi-phase or PSK carrier are in-phase, current flows through one of the two inner loop transistors creating a voltage drop across R24. An out-of-phase relation causes current flow through a side of the outer loop. For discussion purposes, consider that all six transistors in the synchronous detector are biased at the conduction threshold. The $VCO/_2$ input to Q9 is limited between +8.6 and +7.4 by diodes CR12 and CR13, and the limited reference carrier varies from -11.4 to -12.6 volts. When the $VCO/_2$ and the carrier are both at their peaks (-8.6 and -11.4V) together, Q9 is off, Q10 is on, Q13 is on, and Q14 is off. Current cannot flow through either outer loop side under these conditions, therefore Q13 pulls current through Q11 causing a voltage drop across R24. When the $VCO/_2$ and the limited carrier are out of correspondence, (one high, the other low), current flows in one of the outer loop sides. For example, assume that the $VCO/_2$ is at -8.6 volts and the limited carrier is at -12.6 volts. In this case, Q9 is off, Q10 is on, Q13 is off, Q14 is on. Since Q10 and Q14 are both on, current flows in this outer loop side and no current flows in the inner loop so that the Q11 and Q12 collectors are at -8 volts. It is evident that the synchronous detector output voltage is a direct function of the $VCO/_2$ and the reference carrier phase relationship. The demodulated and converted PSK and Bi-phase carrier is fed to the Data Loop where the NRZ family data is integrated and bit detected. This output is limited between ±0.6 volts by diodes CR16 and CR17.

4-42. INTEGRATOR/RESET. The integrator develops a ramp voltage, the amplitude and polarity of which is determined by the input signal and the circuit parameters. The integrator waveform is fed to the bit detector which regenerates the DATA synchronously with the clock.

4-43. Data from the dc restorer goes through emitter follower Q1 to the soft limiter diodes CR2 and CR3 and Q2. The integrator consists of two sets of paralleled current sources connected in opposition. The positive current sources being Q5 and Q7; the negative, Q6 and Q8. The circuit values chosen are such that with the base of Q2 at ground, and R13 properly adjusted, the currents from the opposed sources are balanced. Under these conditions, no current is supplied to the integrating capacitor located in the GPD-6/TU. When the incoming data applied the base of Q29 goes plus, its collector goes minus decreasing the current supplied by Q6 and Q8 allowing Q5 and Q7 to charge the integrating capacitor plus. Negative excursions on the base of Q2 cause Q6 and Q8 to demand more current than the fixed amount from Q5 and Q7. This current is taken from the integrating capacitor causing it to assume a negative voltage. If the data input is a square wave the rise and fall of this voltage will be linear resulting in a triangular waveform. It is desired, however, to integrate over each data bit period therefore the integrating capacitor is reset to zero at the end of each bit period. This is accomplished by the RESET circuit.

4-44. The RESET circuit consists of a one-shot, actuated by the VCO, that clamps the integrating capacitor to ground at the end of each data bit period. The one-shot includes Q11 and Q12 with the timing capacitor located in the GPD-6/TU plug-in. The one-shot is turned on by the differentiated positive going edge of the VCO waveform through C9. Q11 is turned on causing its collector to come down. This allows the junction of R26 and R27 to go negative thus turning on Q12. When Q12 is turned on its collector rises to ground. The timing capacitor tied to the collector of Q12 pulls the junction of R24 and R25 up, back biasing diode CR15, allowing R23 to continue holding Q11 on as initiated by the spike from C9. Both transistors are thus held on until R24 and R25 have pulled their end of the timing capacitor down to the point where CR15 catches the base of Q11 pull it down thus turning it off. Turning off Q11 allows its collector to rise turning off Q12 through R26. The turned on period is determined by the capacitor in the GPD-6/TU and R24-R25. The emitters of Q11 and Q12 are held below and above ground respectively by the CR11, R18 and CR12, R19 networks. The result is that the junction of CR9 and CR10, the integrating capacitor, is clamped to ground through CR9-Q11 if it had been plus, or to ground through CR10-Q12 if it had been minus.

4-45. BIT DETECTOR/DATA DRIVERS. The integrated data signal is fed through emitter follower Q11 to the Bit Detector where a square data wavetrain is restored. The Bit Detector/Data Driver consists of current switch Q12-Q13 and flip-flop Q14-Q15, collector-base coupled by two current driver transistor pairs. The current switch provides set and reset pulses to the flip-flop and is operated by a differentiated VCO pulse fed to both emitters; the integrated data waveform is fed to Q12 base. Current through the switch flows only when the VCO spike occurs, since both transistors are biased at cut-off. When the integration voltage is positive, the VCO spike causes current to flow momentarily through Q13, when the integration voltage is negative, current flows mementarily through Q12 at VCO spike time. Diodes CR18 and CR19 limit the Q12 base input to -0.6 volts. The flip-flop, consisting of Q14-Q15, and current drivers Q16-Q17, Q18-Q19, is triggered by momentary current through one of the transistors of the current switch. The restored data wavetrain may be converted to $\overline{\text{data}}$ by taking the output from the other side of the flip-flop; the front panel INV pushbutton switch selects the side of the flip-flop used.

4-46. CODE CONVERSION.

4-47. The Code Converters illustrated in drawing TY-015731 are located functionally at the output of the Bit Detector/Reset and output lines. As noted in the discussion of the Integrator/Bit Detector, the output data and $\overline{\text{data}}$ lines from the bit detector contain NRZ-L, NRZ-S, NRZ-M or RZ code format depending on the input format selected by the front panel Format and Mode Swtiches. Data bit formats NRZ-L, NRZ-M, NRZ-S or RZ are fed into the Code Converter, and after code conversion, the output data with matching coherent output clock is switch-selectable NRZ-L or RZ. Functional descriptions of all Code Converters follow a discussion of the flip-flop operation and voltages. This is included as an aid to understanding the timing diagrams and logic circuitry.

4-48. FLIP-FLOP TERMINOLOGY AND THEORY. The flip-flop shown in Figure 4-5 is a controlled, bistable circuit which changes state whenever its set or reset conditions are satisfied. The following is a discussion of these conditions, together with an analysis of the flip-flop.

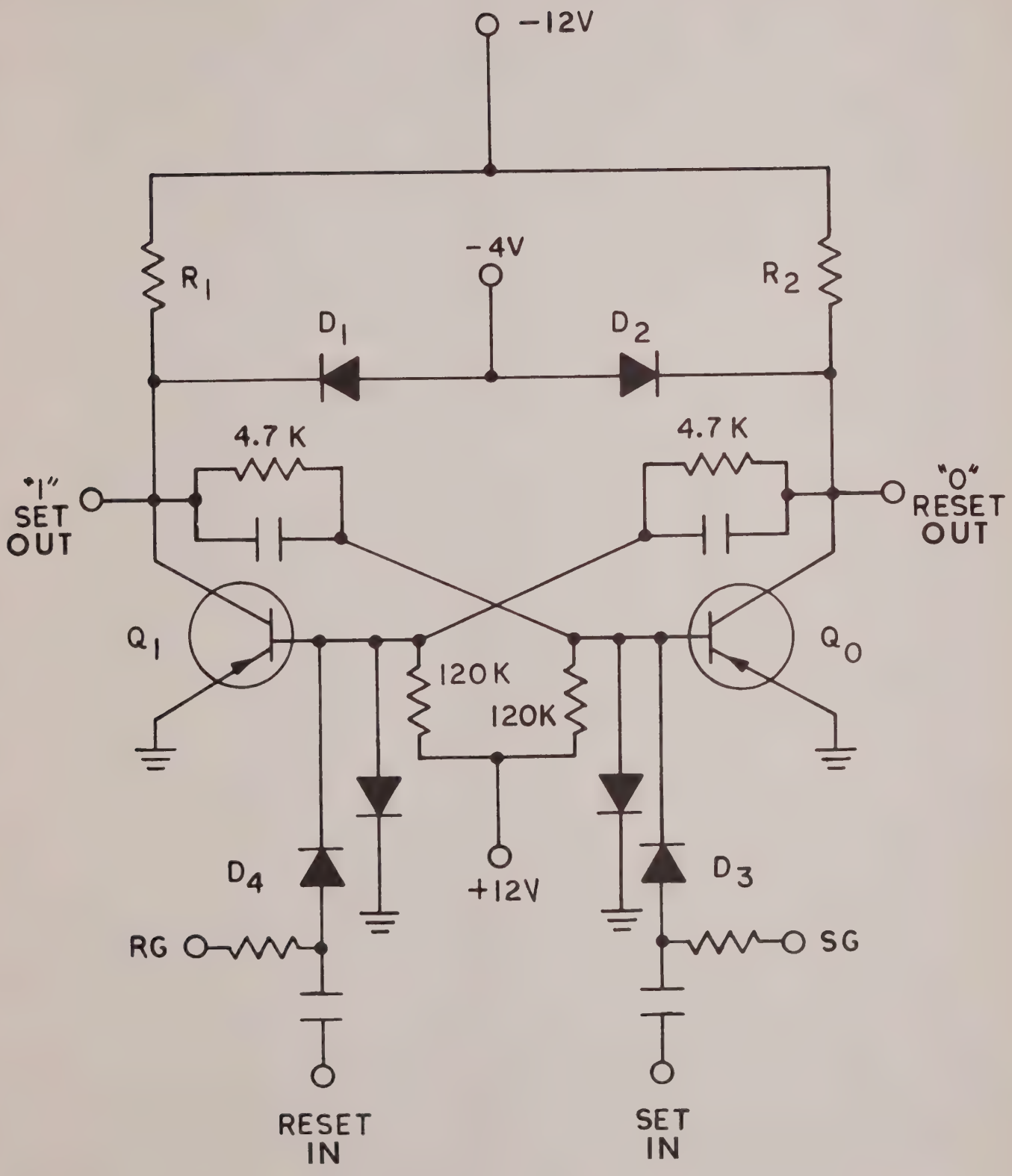


Figure 4-5. Flip-Flop Circuit

4-49. Consider as the initial conditions that Q_1 is saturated and Q_0 is non-conducting, meaning that Q_1 is a short circuit to ground and Q_0 is an open circuit. Theoretically, the entire -12 volt supply is dropped across R1, maintaining the Q_1 collector at 0 volts. With Q_0 an open circuit, its collector is at -12 volts, but diode D2 and the -4 volt bias clamp the Q_0 collector at -4 volts. These conditions define the flip-flop in the set state, with Q_1 collector at 0 volts and Q_0 collector at -4 volts, or a binary "1" at Q_1 and a binary "0" at Q_0. Since both transistors are PNP, a positive pulse at either base will turn that transistor off. If the reset gate happens to be at -4 volts, a reset pulse of +2 volts will not be transmitted through D4. However, if the reset gate is at 0 volts, a reset pulse of +2 volts will forward bias D4 and be applied to the base of Q_1, turning Q_1 off. Note that the reset gate must be at 0 volts before the appearance of a +reset pulse; coincident +2 positive pulses of reset gate and reset terminal will not accomplish turn-off because of the circuit response time. As Q_1 turns off, its collector voltage drops immediately toward -12 volts, but is caught at -4 volts by diode D1 and the -4 volt bias. This voltage drop is coupled to the base of Q_0, and being a negative pulse, will rapidly drive Q_0 to saturation. The Q_0 collector is now at 0 volts and the Q_1 collector is at -4 volts; this condition defines the flip-flop in the reset state with a binary "0" in Q_1 and a binary "1" in Q_0. Setting the flip-flop is accomplished in a similar manner except that the set gate must now be at 0 volts before the appearance of a +2 volt set pulse. This will restore the flip-flop to the original state; a "1" is at Q_1, and a "0" at Q_0 defining the flip-flop set state.

4-50. Referring to the logic block diagram in drawing TY-015731, FF-A has two set terminals, both operating in the same manner as previously described. The set and reset gates of FF-C, FF-D, and FF-E are controlled by AND gate voltages, and those of FF-F are controlled by the output of the flip-flop itself. No matter what the circuitry, the set gate or reset gate must be at 0 volts before a set or reset pulse appears, otherwise no change of state of the flip-flop will occur.

4-51. All flip-flop inputs and outputs operate between ground and -4 volts. Present conditions determine the next state of the flip-flop; therefore, the flip-flop is always dependent on its own present state as well as that of the associated circuitry.

4-52. CODE CONVERTERS.

4-53. The code converter illustrated in drawing TY-015731 and described in table 4-1 consists of two primary converters. The RZ code converter, consisting of flip-flops A, B, C, D, E and F and associated gates converts the selected input code to RZ format. If RZ output is desired, this converter output is fed directly to the data line driver. If NRZ-L output is desired, then the RZ output of this first converter is put into the NRZ-L code converter, flip-flop G, that converts RZ input to NRZ-L which is now connected to the data line driver. The one exception is the case of NRZ-L input and NRZ-L output. Under these conditions, the output of the bit detector is connected directly to the data line driver by-passing all code converters. A bonus of this fact is that if the controls are set for NRZ-L input and NRZ-L output, any format applied to the input will appear cleaned up at the output. Example: NRZ-M in - NRZ-M out.

4-54. Code conversion routing is determined by switches A, B, C, and D (ganged to the front panel format switch) switches C', D', D'' (ganged to the front panel Mode Switch) and the output code switch (mounted on the line driver card) which selects either NRZ-L or RZ output data. Selection of input data format to the Model GPD-6 and the desired output format, determines which of the code converters is used. Code conversion and routing in the code converters are listed in table 4-1. The individual code conversion is discussed in the following paragraphs.

4-55. RZ TO RZ CODE CONVERTER. Most of the code converter circuitry is used only when the incoming data format is RZ. The converter serves two functions: (1) code conversion, and (2) error detection to restore clock synchronization with data. The second function requires clarification. If the RZ data coming from the bit detector includes erroneous bits due to noise, subsequent data bits may or may not be recognized as valid data format when referred to the restored clock out. Therefore some means must be provided to correct, shift or realign the data to coincide with correct clock phase. Rather than shift the clock phase, the RZ code converter shifts the data phase to agree with the restored clock whenever 2 consecutive data bit errors have occurred. The requirements of 2 consecutive errors is based on the error occurrence probability evaluated at a specific signal-to-noise level.

Table 4-1. Code Converter Code Routing

Input Format (to code converter)	Output Data Format	Code Converter Routing
NRZ-L	NRZ-L	Bypassed to output code switch in NRZ position
NRZ-M and NRZ-S	NRZ-L	Flip-Flop "A", through switches C' and C, Flip "G", switches D', D'', D to output code switches in NRZ position
RZ	NRZ-L	Flip-Flop "B", "C", "D" and "E" through switch C to Flip-Flop "G" through switch D to output code switch in NRZ position
NRZ-L	RZ	Gate D 3 through switches C', and C to output code switch in RZ position
NRZ-M and NRZ-S	RZ	Flip-Flop "A" through switches C', and C to output code switch in RZ position
RZ	RZ	Flip-Flops "B", "C", "D" and "E" through switch C to output code switch in RZ position

4-56. Each time 2 consecutive errors have occurred, the Code Converter looks at the incoming data with respect to a new time phase shifted by 180°, beginning at the occurrence of the second error. Consequently, the next 2 subsequent valid data bits will be considered as errors by the Converter, and a total of 4 errors, counting the first 2 data errors, will have occurred. At the fourth error, incoming data and clock out will revert to their original relationship existing before any errors had occurred, because the incoming data phase will be shifted twice by 180° of incoming RZ bit time for a total of 360°.

4-57. The GPD-6 circuitry considers all incoming data as NRZ; this is the basis for a tuning unit and VCO signal at twice the frequency of the incoming RZ bit rate. Due to the doubled VCO, each RZ data bit is seen by the Converter as an NRZ bit, enabling the Converter to detect errors and time phase changes. Proper clock and data format synchronization is guaranteed by these time phase shifts based on statistical error predictions.

4-58. The following description RZ Code Converter is referenced by the Code Converter block diagram, drawing TY-015731, and the timing diagram, Figure 4-6.

4-59. RZ TO RZ CONVERSION. The purpose of this Converter is to detect errors and, after errors have occurred, to correct the phase relationship of incoming data to CLOCK OUT so that the RZ data out will be properly coordinated with CLOCK OUT. This discussion describes drawing TY-015731 and Figure 4-7. An RZ "0" is indefinite if no "1"s appear. For this reason, an extra long incoming RZ data "0" is not counted as an error; but the following RZ "1" bit will be out-of-phase, so it will count as an error.

4-60. ERROR FREE OPERATION. When operating on valid data, the RZ code conversion functions as follows:

a. RZ "1" TO RZ "1". When an RZ "1" appears, gate 13 goes to 0 volts and remains there in time to allow the positive going $\overline{\text{VCO}}$ to SET FF E. Since the SET side of FF E is tied to its own RESET gate, the next positive going $\overline{\text{VCO}}$ pulse resets FF E yielding an RZ "1" in phase and correspondence with the CLOCK OUT.

b. RZ "0" TO RZ "0". The incoming RZ "0" is a quiescent state, consequently no DATA out will be generated.

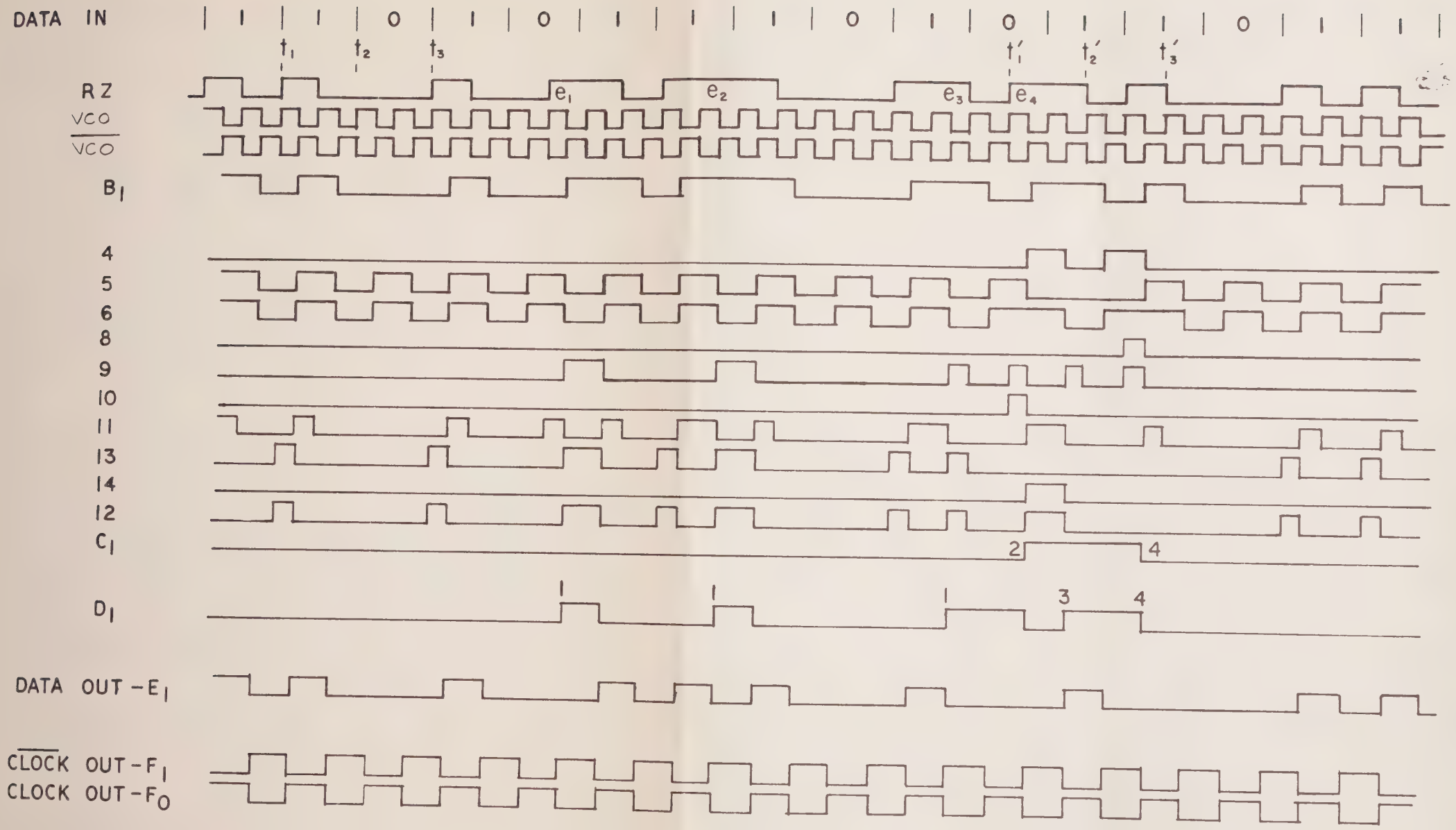


Figure 4-6. RZ to RZ Timing Diagram.

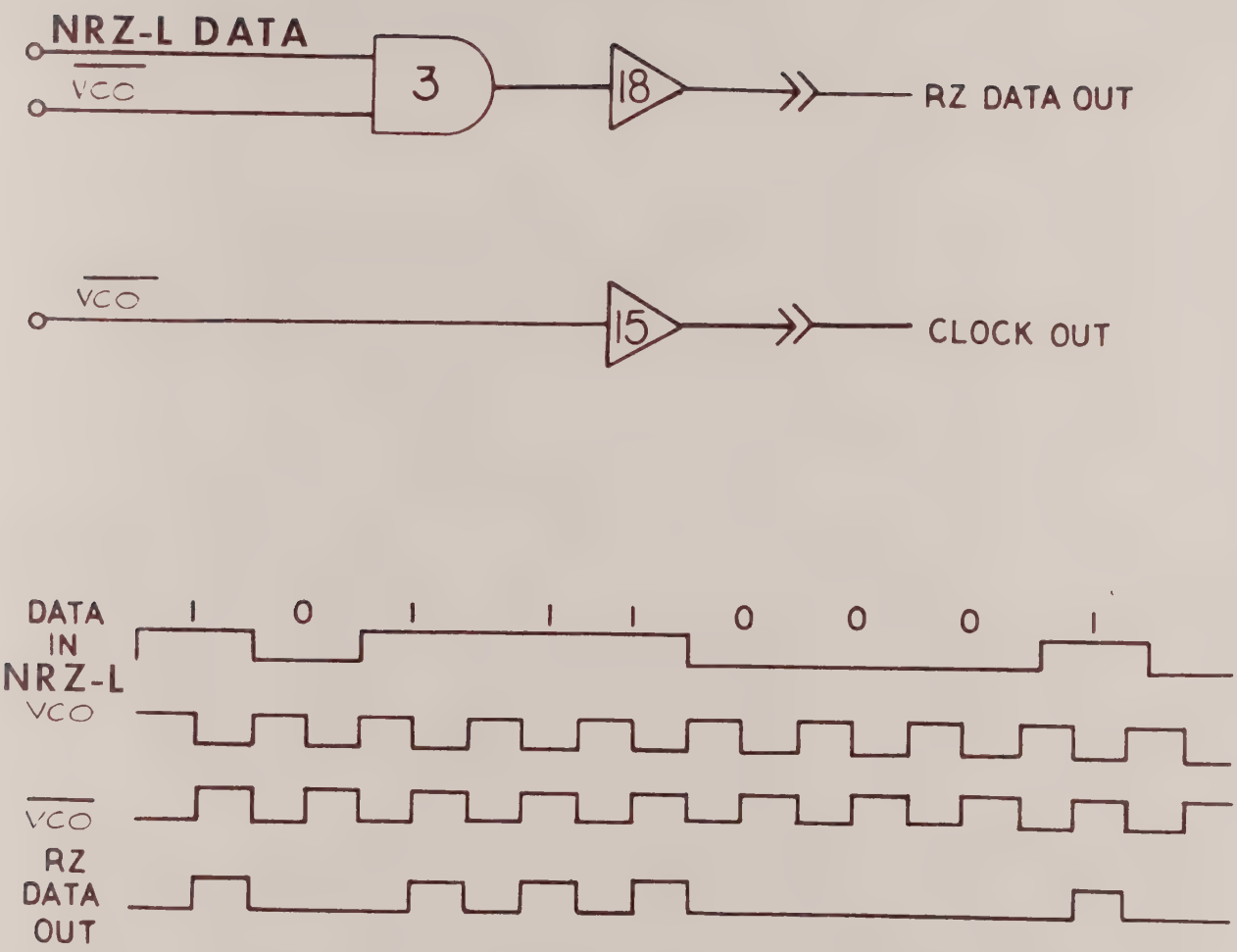


Figure 4-7. NRZ-L to RZ Code Converter/Timing Diagram

4-61. OPERATION WITH RZ DATA ERRORS. Detection of errors in the RZ mode results from a combination of logic circuitry, shown in the code converter diagram. Gates 4, 5, and 6 represent the time base or phase controller for the storing of errors and the phase correction. Gates 8, 10, and 11 are controlled by gate 6, and FF C and FF D (error counters) are controlled by gates 8, 9, 10 and 11. FF B is a buffer which reproduces the incoming RZ data format delayed by 90° of bit time.

4-62. Data bit errors can occur at the second half cycle of an RZ "1" bit, or at the second half cycle of an RZ "0" bit. Whichever the error may be, gate 6 will be up at either of these times. Referring to the timing diagram, e_1 sets FF D. However, e_1 is followed by a valid RZ "1" so FF D is reset by gate 9 due to the RZ "1" and the set side of FF D. Although e_2 is the second error it does not directly follow e_1 and therefore merely begins a new count by setting FF D as e_1 did. Following e_2 is a valid RZ "1", and FF D is RESET again to eliminate the error count.

4-63. Error e_3 again sets FF D, but it is followed immediately by e_4 so that the following sequence occurs. Gate 9 goes up as before, whenever FF D is SET add whenever RZ data is up, but now gate 6 is also up to allow gate 10 to go up. Gate 10 sets FF C which initiates the gate 6 control transfer from gate 5 to gate 4. The transfer keeps gate 6 up and extra 180° of RZ bit time, which is equivalent to shifting the time base of the RZ data 180° with respect to the CLOCK OUT, or 360° with respect to the $\overline{VCO}$. From this point on, the Converter will consider RZ incoming data bits at t'_1 to t'_2 to t'_3, until 2 more errors are counted. As examples, t'_1 to t'_2 is read as an RZ "1" with a second 1/2 cycle error; t'_2 to t'_3 is an RZ "0" with a second 1/2 cycle error. Therefore, 2 more errors have been counted and the fourth error count is recorded by resetting FF D and FF C. Control of gate 6 is reestablished by gate 5 as soon as FF C is RESET telling the Converter that it has shifted the time base by another 180° of bit time, and restoring the original phase relationship of incoming data and CLOCK OUT.

4-64. If more incoming data errors should occur before t'_3, these errors will be counted by alternately setting and resetting FF D. FF C will not be RESET until 2 valid RZ bits have been counted. The reason for this is the elimination of ambiguity from DATA OUT, and the statistical error prediction based on specific signal-to-noise levels. At time t'_3, a valid RZ "1" bit has been eliminated from DATA OUT as a consequence of the gating and timing within the Code Converter.

4-65. NRZ-L TO RZ CONVERSION. This section of the Code Converter is simply AND gate 3, which has inputs of NRZ-L data and $\overline{VCO}$. The output of gate 3 is RZ data which is now in phase and coordinated with the $\overline{VCO}$ used here as the CLOCK OUT. Refer to drawing TY-015731 and Figure 4-7 for the logic circuit and timing diagram.

4-66. NRZ-L "1" TO RZ "1". The NRZ-L "1" bit is twice the width of an RZ "1" and its pulse width is one full clock cycle. Conversion is obtained by use of gate 3 which has ground level output voltage only during the 1/2 period when the $\overline{VCO}$ is at ground.

4-67. NRZ-M AND NRZ-S TO RZ CONVERSION. Refer to the logic and timing diagrams, drawing TY-015731 and Figure 4-8. In the NRZ-M mode, each transition of data represents a "1" whether the change is from positive to negative or negative to positive. The NRZ-M to RZ conversion is accomplished by FF A alone. NRZ-S data transitions occur at a "0" instead of a "1". Conversion to RZ is also accomplished by flip-flop "A".

4-68. NRZ-M "1" TO RZ "1". FF A has NRZ-M and NRZ-M SET inputs, a positive going pulse on either SET terminal will SET the flip-flop in conjunction with the $\overline{VCO}$. The next positive going $\overline{VCO}$ will RESET FF A to convert NRZ-M to RZ. (NRZ-S to RZ is of course similar).

4-69. RZ TO NRZ-L CONVERSION. Discussion of this Converter is referenced by Figure 4-9. RZ output data from the RZ Converter is used together with $\overline{VCO}$ to drive FF G. The RZ output data is used as a SET gate and $\overline{RZ}$ is used as a RESET gate. The inverted $\overline{VCO}$ positive going pulses trigger the flip-flop for either SET or RESET conditions.

4-70. RZ "1" TO NRZ "1". Assume FF G is in the RESET state. When an RZ "1" appears, the first positive going $\overline{VCO}$ will SET FF G 180° after the RZ "1". FF G cannot be RESET until a positive going $\overline{VCO}$ pulse occurs during an RZ "0". This means that FF G remains SET for one complete NRZ bit time, yielding an NRZ "1". FF G is RESET by a $\overline{VCO}$ positive pulse and $\overline{RZ}$ data; $\overline{RZ}$ data coincides with a $\overline{VCO}$ pulse only during RZ "0"s.

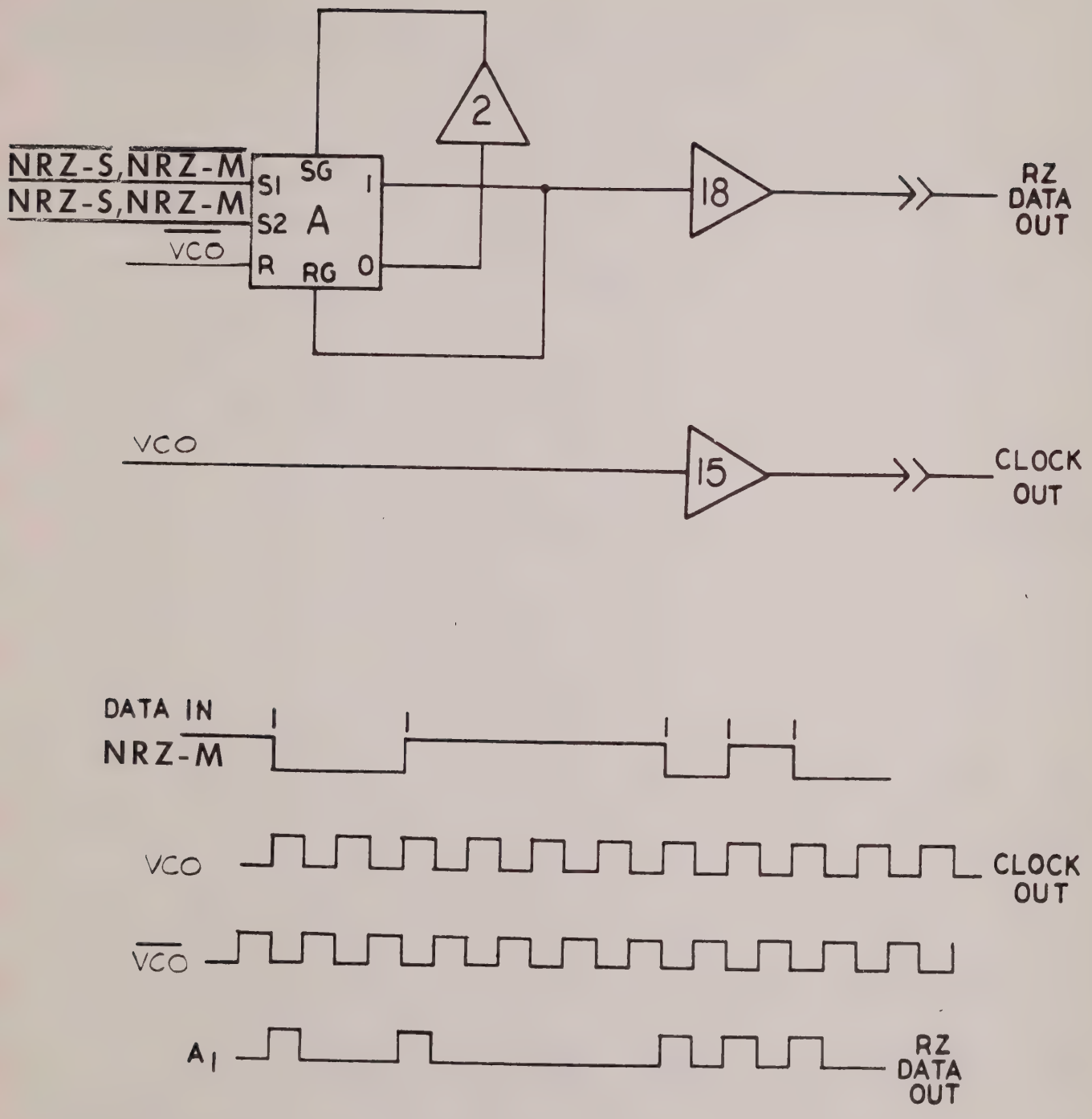


Figure 4-8. NRZ-M/NRZ-S to RZ Code Converter/Timing Diagram

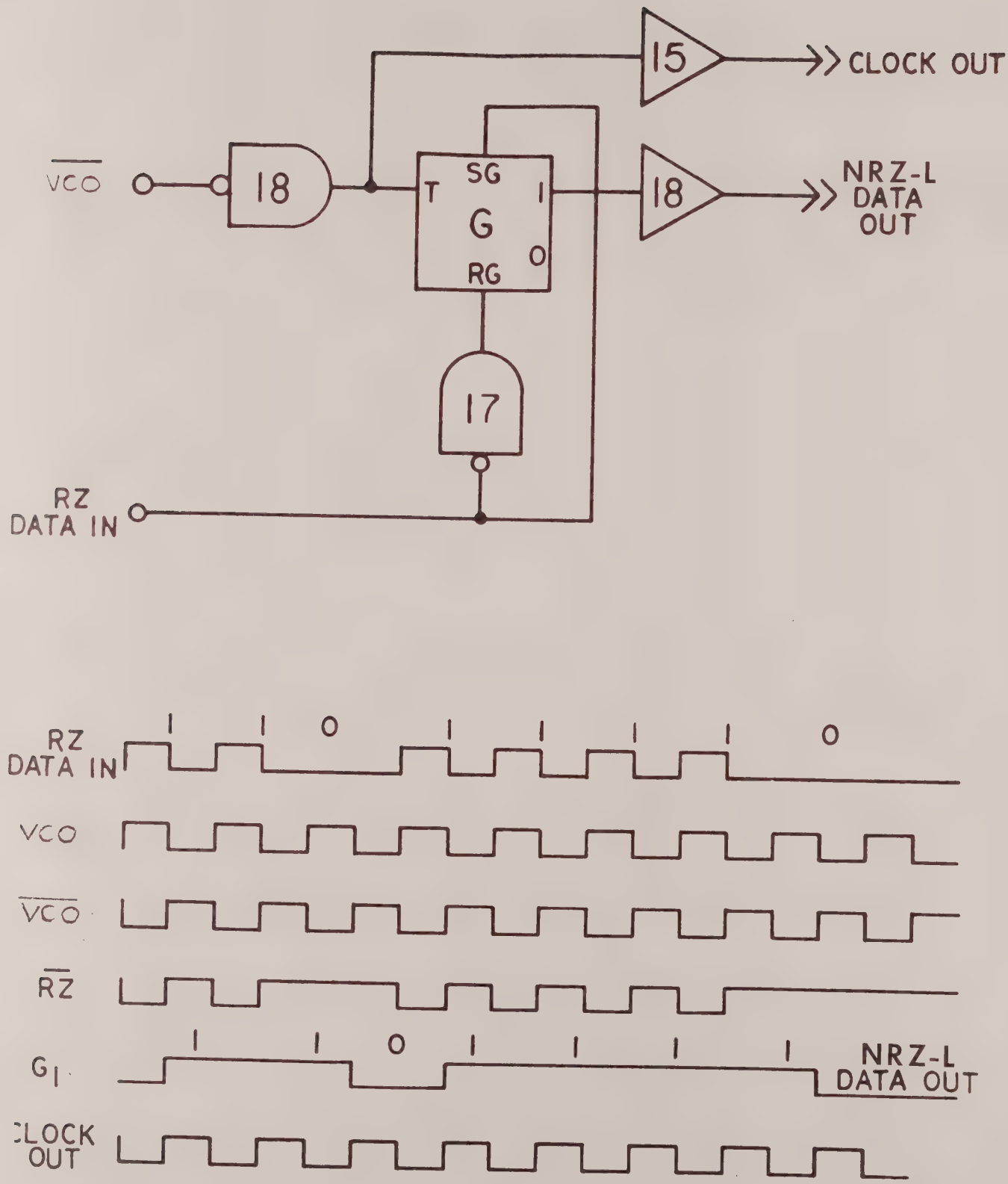


Figure 4-9. RZ to NRZ-L Code Converter/Timing Diagram

4-71. NRZ-M and NRZ-S to NRZ-L CONVERSION. This conversion is accomplished in two sequences: First, the NRZ-M or NRZ-S is converted to RZ format in flip-flop A, which is discussed in NRZ-M to RZ conversion (figure 4-8); second, the RZ data is converted to NRZ-L format in flip-flop G, already discussed in RZ to NRZ-L conversion (figure 4-9).

4-72. AND GATE CIRCUIT. Assume the voltages E1, E2, and E3 in the AND gate circuit of figure 4-10 are approximately equal and less than the positive supply voltage. As the diodes are forward biased, the output voltage will equal the lowest voltage plus the diode forward biased, the output voltage will equal the lowest voltage plus the diode forward voltage drop. If the output voltage is defined zero with respect to some voltage level, say E4; E1, E2, and E3 must be greater than E4 to produce a positive output.

4-73. INVERTER CIRCUIT. The inverter Circuit of figure 4-10 is a common collector transistor amplifier operating in the switching mode. When the base potential decreases to permit an increase in emitter-base drive current, the collector current increases to increase and thus invert the output signal. In the absence of an input signal, diode D2 is forward biased to reverse bias the transistor by the voltage drop across D2. With zero input, diode D1 is forward biased holding the output voltage to approximately -4 volts. Resistor R1 provides base current limiting while C1 ensures rapid current rise time by compensating for the transistor junction capacitance.

4-74. POWER INVERTER CIRCUIT. The Power Inverter of figure 4-10 uses an extra transistor Q3 to secure an actual rather than an effective reversal of output current. With zero input signal, the +12 volt supply reverse biases Q2 to the non-conducting or cut off condition. With Q2 cut off, Q3 is forward biased and current flows through Q3 to the -4 volt supply. When the input signal decreases, Q2 is forward biased and the output component of Q2 current flows through D3 to the output. Note that the forward voltage drop across D3 reverse biases Q3 to the cut off condition. The parallel R-C circuit performs the same function as R1 - C1 in the Inverter Circuit.

4-75. LINE DRIVER AMPLIFIERS. The Line Driver Amplifiers increase the power level of the Code Converter DATA and CLOCK outputs and provide the proper internal impedance to match the 91 ohm characteristic impedance of RG-62/U coaxial cable. Assuming the coaxial cable is properly terminated in 91 ohms, the impedance match preserves the GPD-6 rise-time characteristics and maximizes the available output power.

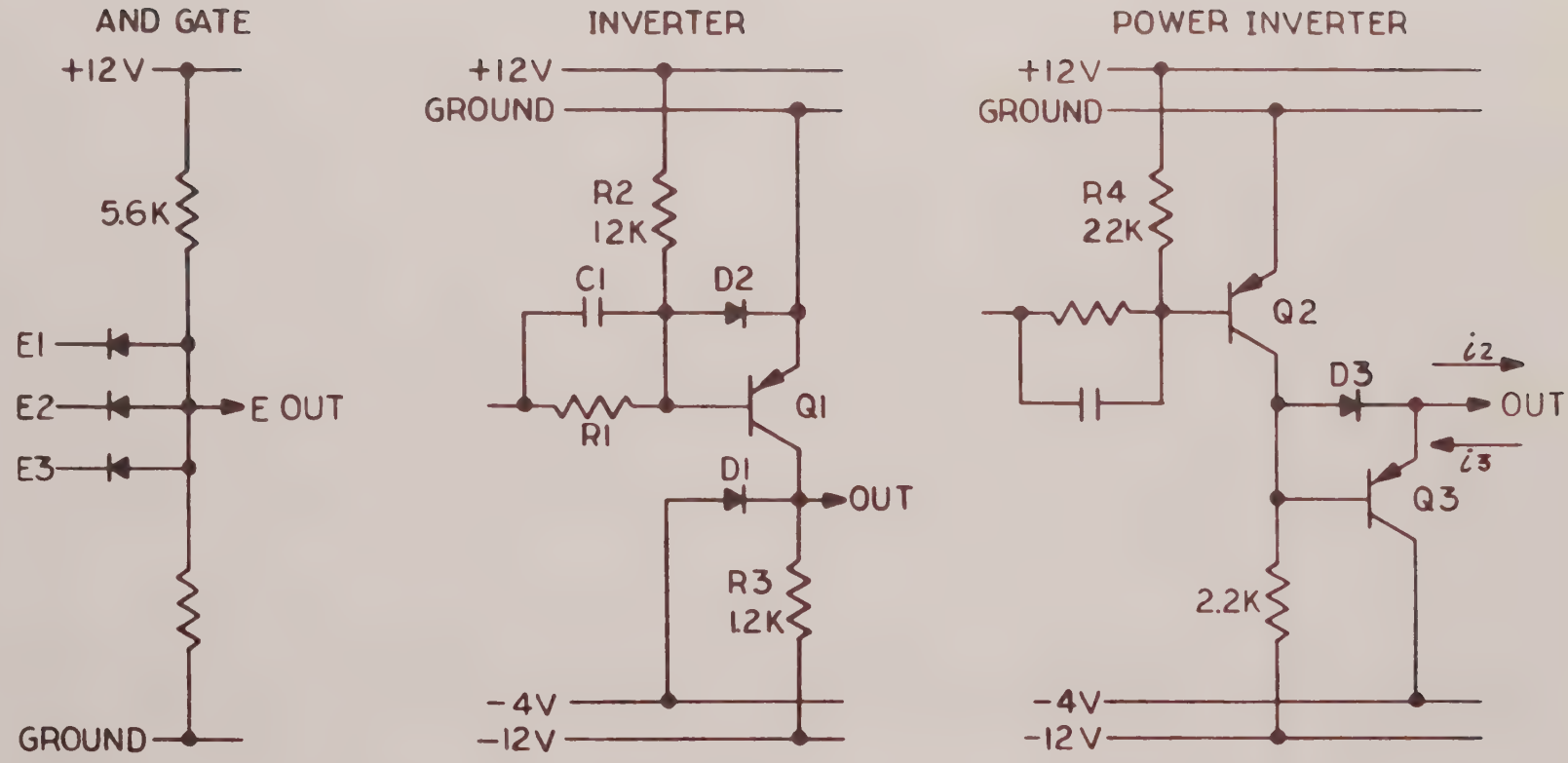


Figure 4-10. AND Gate, Inverter and Power Inverter

4-76. The input to the Line Driver Amplifier is through the emitter-follower Q1 (see figure 4-11). The base and hence the emitter swings between ground and -4.5 volts (approximately). The zener SV1 serves as a low impedance level changer of approximately 7 volts. The junction of SV1 and R1 and the base of Q2 therefore, swing between -7V and -11.5V. The base of Q3 is pegged at approximately 10 volts by the emitter of Q4 as determined by R6 and R7. When the base of Q2 is at -11.5V no current flows through it because its emitter is held at -11V by Q3. All current through R4 flows through Q3 and output resistor R3. When the base of Q2 goes to -7 volts Q2 is turned on and Q3 is turned off- all current from R4 flowing through Q2 and R2. Output across R3 drops to zero. The output taken across R3 is set by the voltage on the base of Q3 and the value of R4. This is approximately 6 volts at the impedance set by the value of R3- 90.9 ohms.

4-77. Transistor Q4, also in the emitter-follower configuration, acts as a regulator to provide a fixed base potential and therefore quiescent base polarizing (bias) current for Q3.

4-78. FREQUENCY METER. The Metering Circuit (figure 4-12 and drawing BD-015291) compares the VCO frequency with the data signal to generate a Frequency-Set Meter signal roughly inversly proportional to the frequency difference. In the presence of severe noise or data signal fading sufficient to disrupt the phase-lock-loop, the metering circuit produces an indication of loss of phase lock. Switching is included to permit open loop fine adjustment of the GPD-6 tuning circuits during actual data signal reception.

4-79. The triangular VCO signal is clipped on top and bottom by diodes CR1 and CR2, and amplified by the Q3401 inverter. Q3402 and Q3403 are connected as a Schmitt Trigger to square up the clipped and amplifier VCO signal which now appears as a square wave at the Q3403 collector. The frequency of this square wave is the original VCO signal frequency. The squared VCO signal is inverted once by Q3404, and inverted again by Q3405 to provide two identical signals 180° out of phase with each other. The Q3404 and Q3405 outputs are the SET and RESET signals respectively, for the flip-flop consisting of Q3406 and Q3407. DATA taken from the Doubler output of the GPD-6 is inverted by Q3408 and applied to the SET gate and RESET gate to the flip-flop.

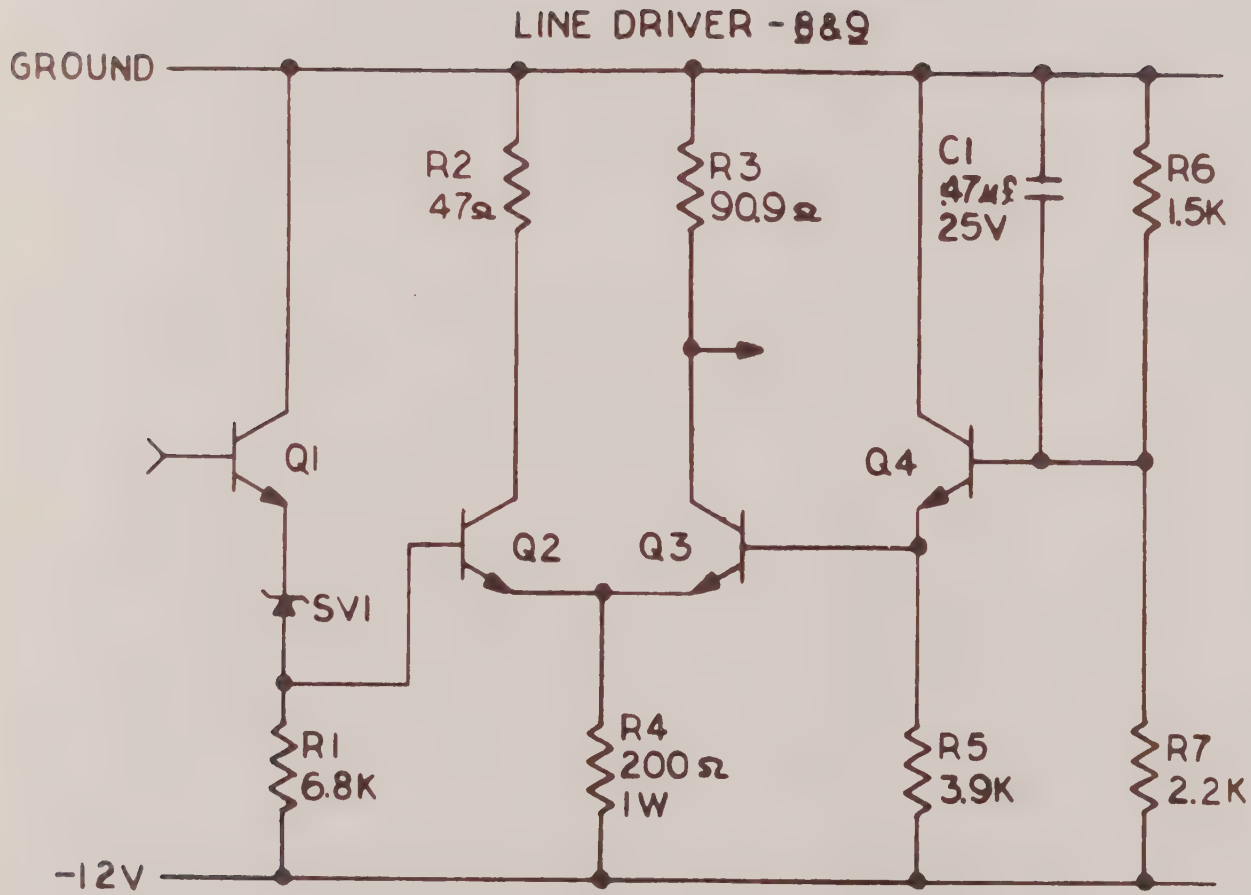


Figure 4-11. Line Driver Amplifier

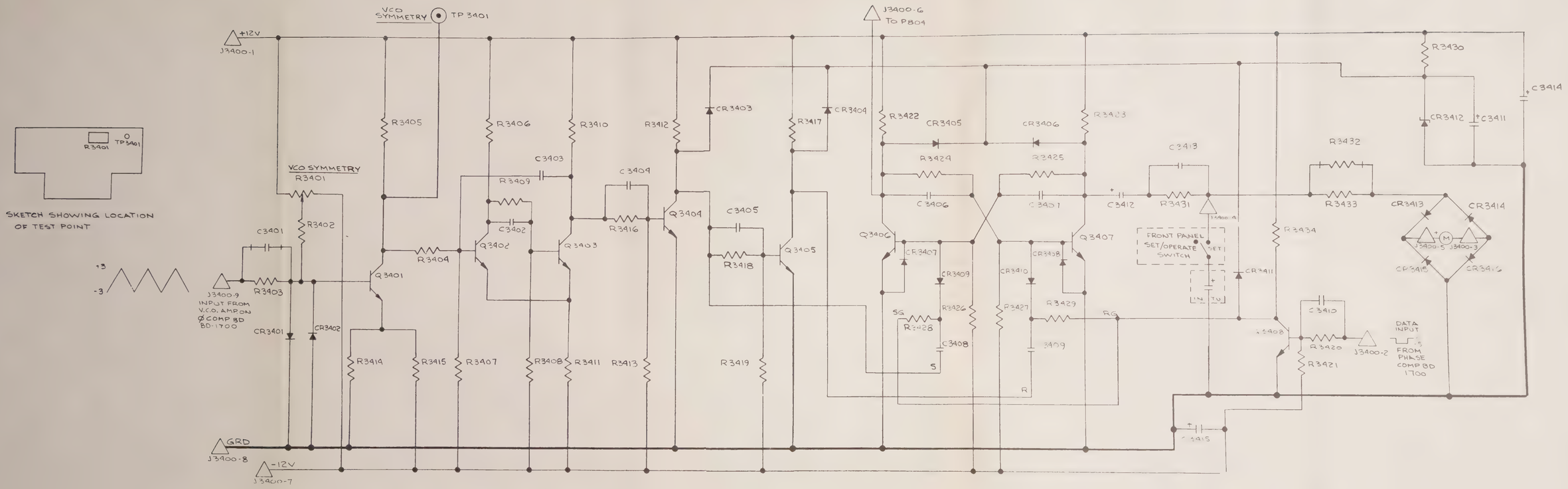


Figure 4-12. Metering Circuit

4-80. When the GPD-6 is in lock, the VCO signal and DATA correspond to phase and frequency so that the fixed relationship of SET, RESET and SET gate, RESET gate can not make the flip-flop change state. As a result, C12 remains charged to the d-c voltage obtained at the Q3407 collector and no current flows in the meter or diode bridge.

4-81. As the DATA rate begins to "slip" with respect to the VCO rate, Q6 and Q7 begin to change state since their set and reset inputs (VCO) no longer have fixed phase relationship with the set and reset gates (DATA). Consequently, the flip-flop changes stage at a rate proportional to the difference in VCO and DATA rate. C12 charges and discharges according to the voltage change at the Q7 collector, and the current produced is rectified by the diode bridge causing deflection of the meter. Since the meter detects average current, its deflection will be proportional to the severity of loss-of-lock in the GPD-6 phase lock-loop. Full meter deflection indicates complete loss of lock. At small differences of VCO and DATA rates the meter deflection will oscillate due to the slow charge and discharge of C12. As the frequency difference becomes greater, the meter deflection tends to stabilize at the average current magnitude. Either noise or out-of-lock conditions may cause a meter deflection.

4-82. To adjust the tuning unit to the VCO center frequency, the Phase-Lock-Loop is opened when the Mode Switch is in the SET position. In the SET position, a capacitor located in the Tuning Unit is a low pass filter for the Q3407 output. At the VCO center frequency, the Q3407 output causes full meter deflection because of the low pass capacitor. As the VCO approaches its center frequency, the meter approaches full scale. Detuning the VCO results in meter oscillations representing the frequency difference from the center frequency.

4-83. PHASE ERROR OR LOOP STRESS METER. The function of this meter has been previously discussed in the DC AMPLIFIER/LOOP FILTER section.

4-84. PRIMARY POWER SUPPLIES. The basic positive and negative power supplies are identical full wave rectifiers with simple capacitor (C11 and C22) filters. Resistors Rb1 and Rb2 are bleeder resistors to discharge the filter capacitors when the unit energizing source is removed. See figure 4-13 for Power Supply Circuits.

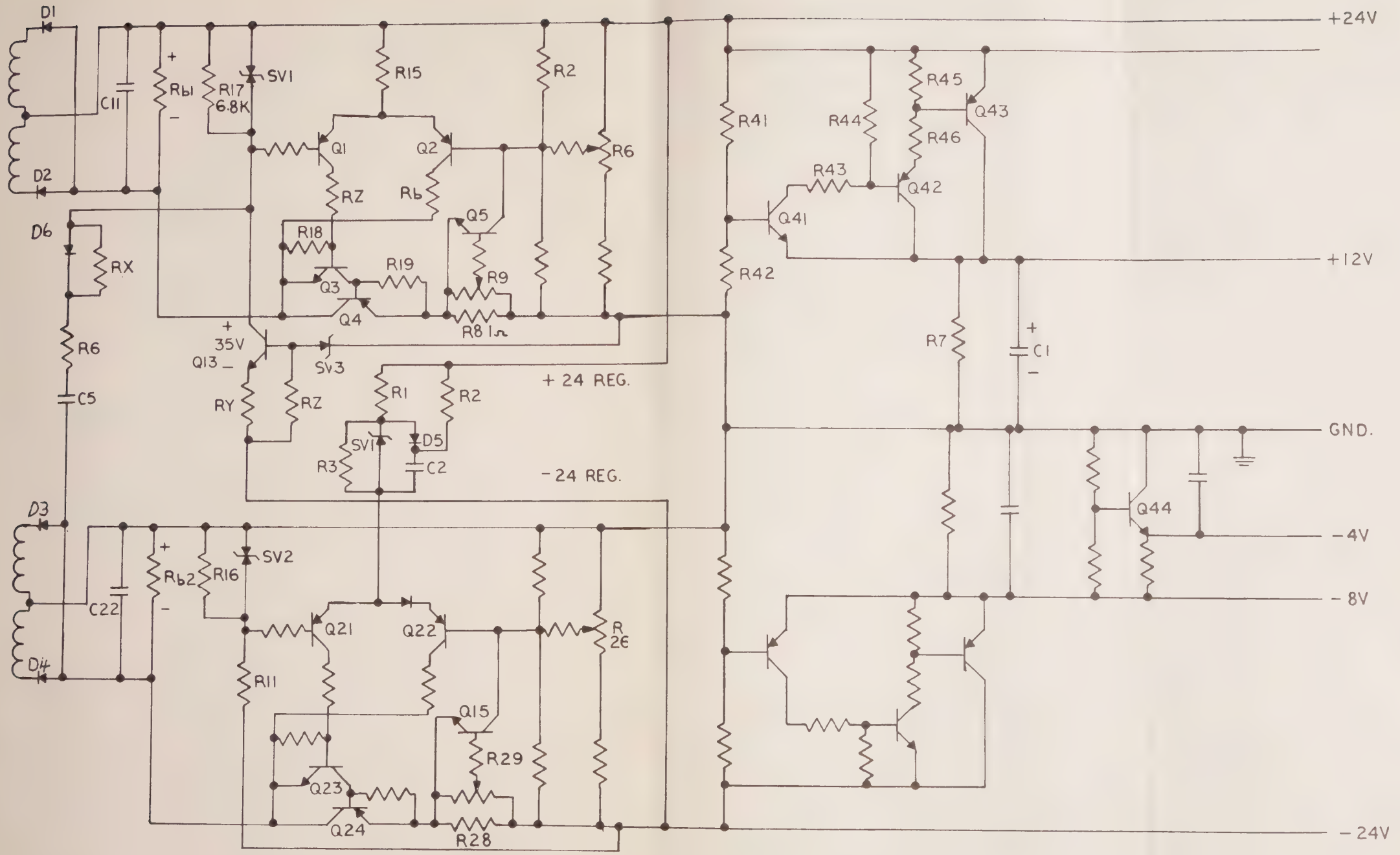


Figure 4-13. DC Power Supplies

4-85. PRIMARY POWER SUPPLY REGULATOR CIRCUITS. The Primary Regulator Circuits minimize the ripple voltage of the full wave rectifier circuits and maintain constant ±24 output voltages under normal line and load variations. The 24 volt output also serves as a source for the lower voltage regulator circuits.

4-86. Assume that both regulators are operating normally and a circuit fluctuation tends to change the positive regulator output to +25 volts. The increase in voltage across R2 increases the forward bias on Q2 and therefore the Q2 collector current in R15. Since the Q1 base potential is fixed by the symmetrical regulator diode (SV1), the increase in R15 voltage reduces the Q1 forward biasing current. The resultant decrease in Q1 collector current reduces the Q3 drive current which in turn reduces the drive to transistor Q4. As the Q4 emitter-base drive current decreases, the voltage across Q4 increases to offset the increase in output voltage.

4-87. In a similar manner, the 1 ohm current sensing resistor R8 and transistor Q5 provide output current overload protection. Potentiometer R9 in parallel with R8 is adjusted to maintain Q5 cut off for all currents below a predetermined value. If a fault occurs to produce greater than twice normal load current, the voltage increment developed is sufficient to forward bias Q5. With Q5 forward biased, the Q5 collector current component in the Q2 emitter-base circuit controls Q2 to reduce the output voltage and therefore the output current.

4-88. Potentiometer R6, by varying the Q2 emitter-base current, permits a fine adjustment out the output voltage.

4-89. SHORT CIRCUIT PROTECTION. The Short Circuit Protection is derived from a cross coupling between the 24 volt regulators such that the input or output condition of one determines the output of the other. If the output of either regulator is appreciably reduced by an external or an internal circuit malfunction, both regulators will be turned off. The regulators will remain off until the entire power supply is deenergized for a period of several seconds and then reenergized.

4-90. Assume a circuit fault such that the positive regulator output current increases rapidly above a value set by R9 (see paragraph 1-157). As (indirectly) Q5 lowers the positive regulator output, the Q21 emitter biasing network potential and therefore the Q21 forward biasing current decreases (note that the Q21 base potential is held relatively constant by the SV2 regulator diode). The resulting decrease in Q21 collector current effectively decreases the Q24 drive and therefore the output of the negative regulator. When the voltage on R16 approaches the SV2 sustaining voltage, the decrease in SV2 voltage further reduces the Q21 collector current. The developed positive feedback results in a rapid turn-off of the negative regulator circuit.

4-91. During normal operation Q13 is forward biased by the negative regulator output to carry the Q1 base current in addition to the R17 and SV1 currents. When the decreasing negative regulator output reduces the Q13 forward bias, the Q13 current and therefore the Q1 current decreases to reduce the drive of Q4. Continued decrease of the negative regulator output results in the cut off of Q13, Q1 and Q4. When Q4 is cut off, no current can flow and the negative regulator output is zero.

4-92. Both regulators will now remain off even though the circuit fault is removed. The cross coupling, that is the input of one regulator to the output of the other, forces a zero current condition in one regulator until the other regulator produces a voltage. The rectifier supply voltage does not appear in the regulator circuits as it is fully disconnected by the open circuit condition of the series regulator transistors. The regulators may only be re-energized by turning the power supply off for several seconds and then back on.

4-93. As shown above neither plus or minus supplies can be on unless the other is. This means the supplies will not come on when the AC power is first applied or a short removed. This difficulty is overcome by the network consisting of C5, R6, D6 and RX.

4-94. With power off, C5 is not charged. When power is turned on, the full unregulated voltage for the minus supplies appears across C22 and therefore on the lower side of C5. C5 pulls current through R6 and D6 thereby developing a voltage across SV1. A voltage across SV1 allows the +24V supply to turn on. Turning on the +24V supply turns on the -24V supply which will now in turn supply current through Q13 to keep SV1 active. C5 meanwhile charges to the point where it no longer draws current through SV1. In the

event that a short exists on any of the supplies there will be no cross reference voltage and neither supply can come on. The +24V supply will attempt to come on for the duration of the time constant of C5 and R6. RX is relatively in value and is the means of discharging C5 when the power is turned off. D6 is a low impedance at turn on and high impedance when operating.

4-95. SECONDARY POWER SUPPLIES. The Secondary Power Supplies are series regulators to produce minimum output impedance at voltage levels determined primarily by the input voltage divider circuits. Only the +12 volt and the -4 volt supplies will be considered as the remaining units are essentially identical to the +12V supply and -4V supply is unique.

4-96. Assume an output load increase tending to reduce the voltage across the R7 - C1 filter circuit. As the Q41 base potential is approximately constant, the base-emitter forward bias current is increased hereby increasing the Q41 collector current. The emitter-base current of Q42 is proportional to the Q1 collector current and consequently the Q42 current increases. Similarly, the Q42 current increases the forward bias on Q43 thus increasing the Q43 collector current to compensate for the increased load current.

4-97. The -4 volt supply is unique in that it does not supply current to a load that is to ground but rather a load that is connected to -8 volts. This load consists primarily of the collector resistors of flip-flops that are connected to -8V but whose collector ends are caught by diodes to the -4V supply. The -4 volt supply can be considered to be an emitter-follower supplying current to a more negative load.

4-98. GPD-6/BP PLUG-IN. This typical plug-in module is designed for a 1.024KHz center frequency and a maximum bit rate of 70kb. A four-position front panel switch selects the Gain, Input, and Sensitivity as shown in Table 4-2.

Table 4-2. Gain Selection

Switch Position	Max. Input	Max. Sensitivity
OFF	25V pp	.5V pp
X1	7V pp	500MV pp
X3	3V pp	170MV pp
X10	1V pp	50MV pp

4-99. Two basic configurations are available. The GPD-6/BP, (refer to drawings TW-016005 and TA-016003) is a typical narrow-band unit for 1.024 MHz ±55 KHz center frequency. The GPD-6/BP (refer to drawings RA-017476 and GW-017475) is a typical wide-band unit for 1.024 MHz ±260 KHz center frequency. Various center frequencies and band widths are available when specified.

SECTION V

MAINTENANCE

5-1. GENERAL.

5-2. This section provides information, procedures and illustrations to perform preventive maintenance, periodic calibration, performance tests and troubleshooting.

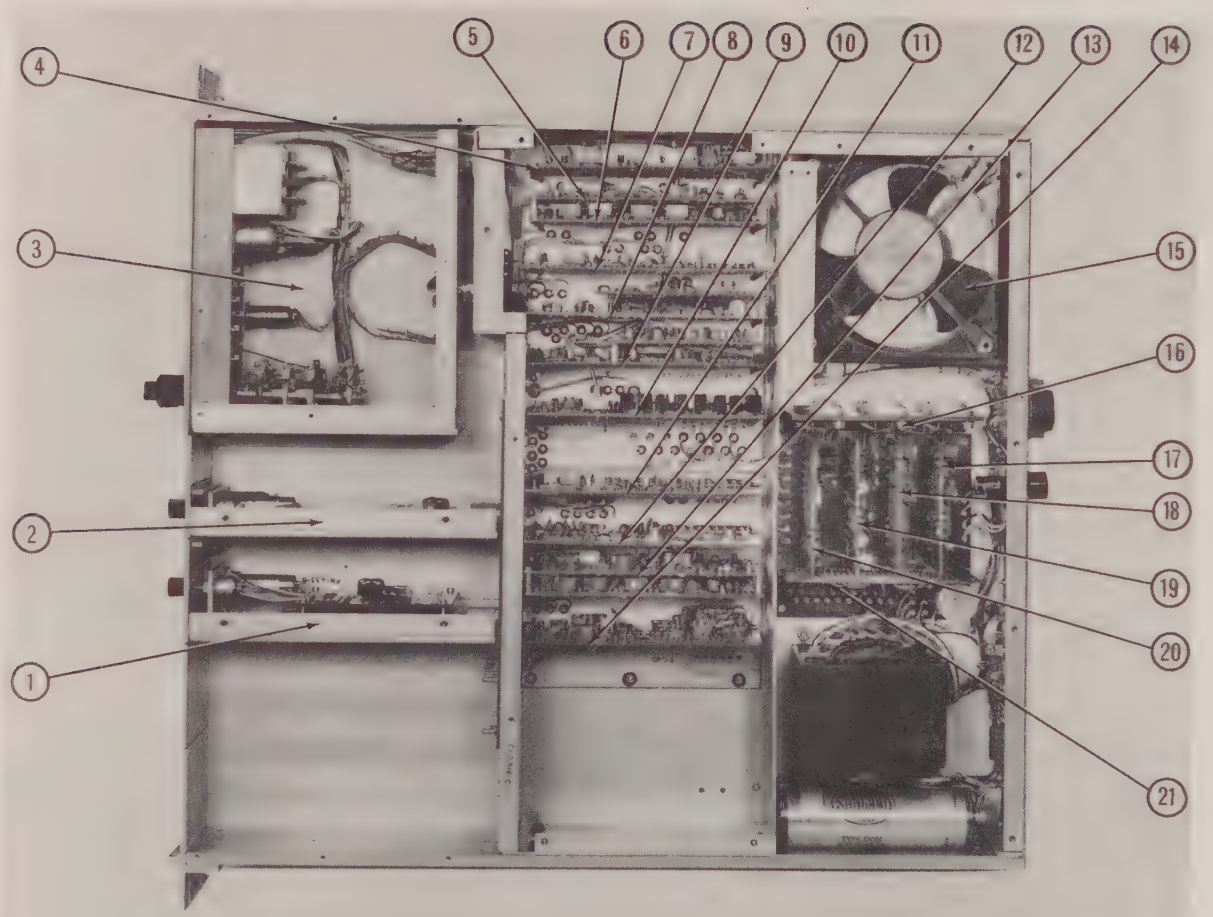
5-3. For easy identification of circuit boards, functions and test points, a captioned photo and two main diagrams are furnished: Figure 5-1 shows circuit board particulars and locations; Figure 5-2 is a maintenance block diagram showing front panel test jacks; and Figure 5-3 is a detailed test point, adjustment pot, connector, and circuit board locator. Drawings of each circuit board showing all component locations are also provided in Section VI.

5-4. Test equipment required is listed in Table 5-1 and each test procedure contains a list of test equipment needed to perform the particular tests.

Table 5-1. Test Equipment

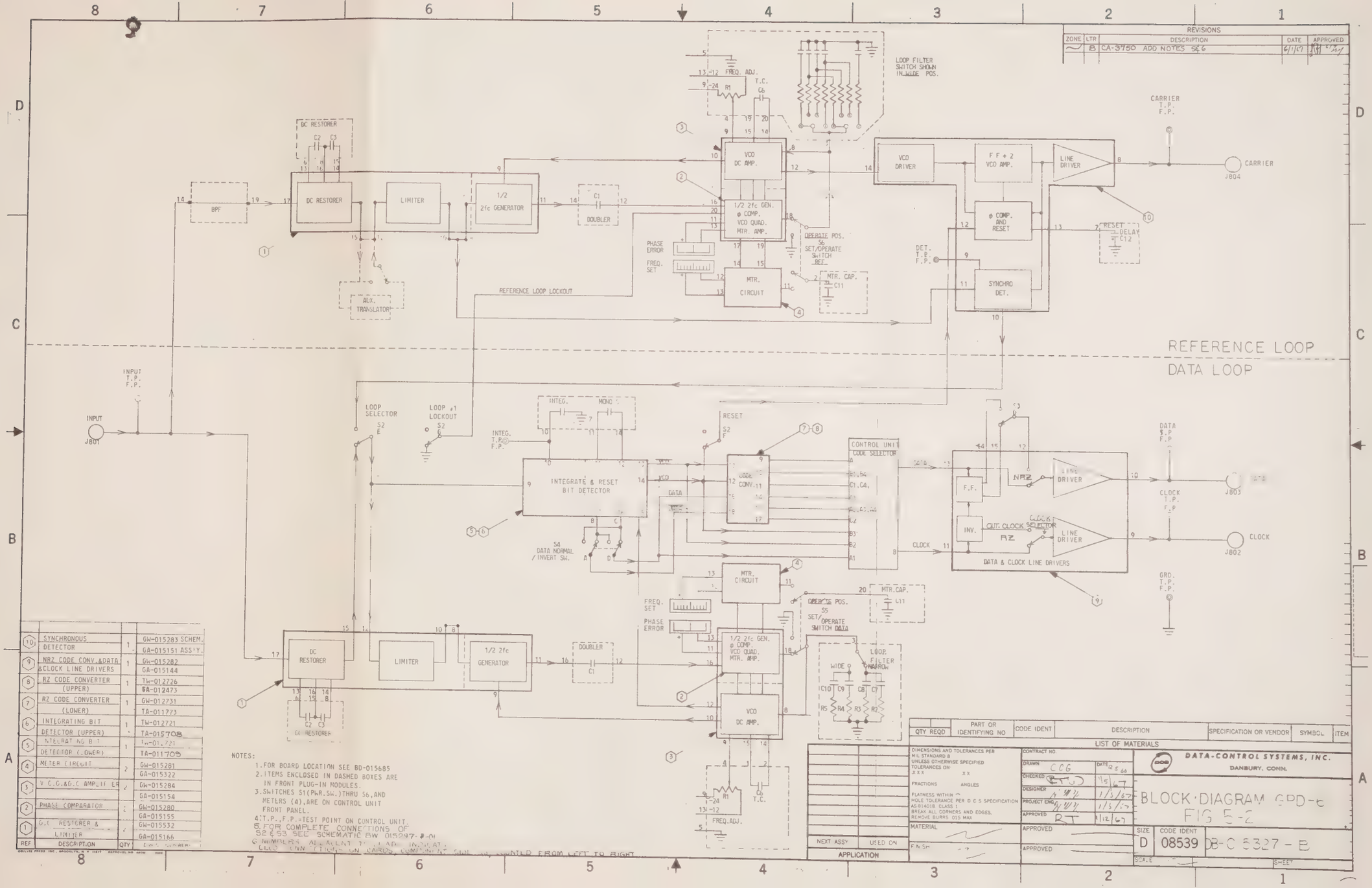
Nomenclature	Characteristics
VTVM	5% accuracy
Dual Trace Scope	Tektronix 545A or equivalent
Random Noise Generator	Scott 811-B, 2 volts out or equivalent
Square Wave Generator	
PCM Digital Simulator	16 Bit Variable Word
Frequency Counter	
PSK Generator	DCS

5-5. SPECIAL TOOLS. No special tools required.



1. GPD-6/F Reference Tun.
2. GPD-6/TU Bit Rate Tun.
3. Control Unit
4. DC Restorer-PCM
5. Phase Comparator
6. VCO-PCM
7. Meter-PCM
8. Bit Detector
9. RZ Code Converter (Lower)
   RZ Code Converter (Upper)
10. NRZ Code Converter-Line Drivers
11. Meter-PSK
12. Synchronous Detector-Line Driver
13. VCO Lower Bd. Phase Comp.-PSK
14. DC Restorer-PSK
15. Fan
16. Regulator Output Transistors
17. Power Supply Card +24V DC
18. Power Supply Card -24V DC
19. Power Supply Card +8V +12 V DC
20. Power Supply Card -4V DC, -8V DC, -12V DC
21. Power Supply, Lamps

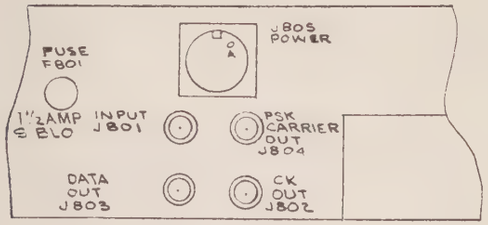
Figure 5-1. GPD-6, Location of Assemblies.


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B | CA-3750 ADD NOTES 5&6 | 6/1/67
REFERENCE LOOP
DATA LOOP
LOOP FILTER SWITCH SHOWN IN WIDE POS.
FREQ. ADJ.
T.C.
DC RESTORER
BPF
LIMITER
1/2 2fc GENERATOR
DOUBLER
AUX. TRANSLATOR
VCO DC AMP.
1/2 2fc GEN. φ COMP. VCO QUAD. MTR. AMP.
MTR. CIRCUIT
MTR. CAP.
OPERATE POS. S6 SET/OPERATE SWITCH REF.
PHASE ERROR
FREQ. SET
REFERENCE LOOP LOCKOUT
VCO DRIVER
F F ÷ 2 VCO AMP.
LINE DRIVER
φ COMP. AND RESET
SYNCHRO DET.
RESET DELAY C12
CARRIER T.P. F.P.
CARRIER J804
DET. T.P. F.P.
INPUT T.P. F.P.
INPUT J801
LOOP SELECTOR S2 E
LOOP #1 LOCKOUT S2 G
INTEG. T.P. F.P.
INTEG.
MONO
INTEGRATE & RESET BIT DETECTOR
CODE CONV.
CONTROL UNIT CODE SELECTOR
RESET S2 F
S4 DATA NORMAL / INVERT SW.
DATA
CLOCK
F.F.
INV.
NRZ
RZ
OUT. CLOCK SELECTOR
DATA & CLOCK LINE DRIVERS
DATA T.P. F.P.
CLOCK T.P. F.P.
GRD. T.P. F.P.
J803
J802
WIDE
NARROW
LOOP FILTER
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10
R1 R2 R3 R4 R5
NOTES:
1. FOR BOARD LOCATION SEE BD-015685
2. ITEMS ENCLOSED IN DASHED BOXES ARE IN FRONT PLUG-IN MODULES.
3. SWITCHES S1(PWR.SW.) THRU S6, AND METERS (4), ARE ON CONTROL UNIT FRONT PANEL.
4. T.P., F.P. = TEST POINT ON CONTROL UNIT.
5. FOR COMPLETE CONNECTIONS OF S2 & S3 SEE SCHEMATIC BW 015297-2-01
6. NUMBERS ALL ADJACENT TO LEADS INDICATE LOGIC CONNECTIONS ON CARDS, COMPONENT SIDE VIEW, VIEWED FROM LEFT TO RIGHT
10 SYNCHRONOUS DETECTOR 1 GW-015283 SCHEM. GA-015151 ASSY.
9 NRZ CODE CONV. & DATA & CLOCK LINE DRIVERS 1 GW-015282 GA-015144
8 RZ CODE CONVERTER (UPPER) 1 TW-012726 GA-012473
7 RZ CODE CONVERTER (LOWER) 1 GW-012731 TA-011773
6 INTEGRATING BIT DETECTOR (UPPER) 1 TW-012721 TA-015708
5 INTEGRATING BIT DETECTOR (LOWER) 1 TW-012721 TA-011705
4 METER CIRCUIT 1 GW-015281 GA-015322
3 V.C.O. & D.C. AMPLIFIER 1 GW-015284 GA-015154
2 PHASE COMPARATOR 2 GW-015280 GA-015155
1 D.C. RESTORER & LIMITER 1 GW-015532 GA-015166
REF | DESCRIPTION | QTY | PART NUMBER
QTY REQD | PART OR IDENTIFYING NO. | CODE IDENT | DESCRIPTION | SPECIFICATION OR VENDOR | SYMBOL | ITEM
LIST OF MATERIALS
NEXT ASSY | USED ON
APPLICATION
DIMENSIONS AND TOLERANCES PER MIL STANDARD 8 UNLESS OTHERWISE SPECIFIED
TOLERANCES ON: XXX ± .XX ± FRACTIONS ± ANGLES ±
FLATNESS WITHIN ○ HOLE TOLERANCE PER D C S SPECIFICATION AS-B1401B, CLASS 1
BREAK ALL CORNERS AND EDGES. REMOVE BURRS .015 MAX
MATERIAL
FINISH
CONTRACT NO.
DRAWN CCG 12 5 66
CHECKED RTD 1/6/67
DESIGNER 1/5/67
PROJECT ENG. 1/5/67
APPROVED RT 1/12/67
APPROVED
APPROVED
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.
BLOCK DIAGRAM CPD-C
FIG 5-2
SIZE D | CODE IDENT 08539 | DB-C 5327-B
SCALE | SHEET

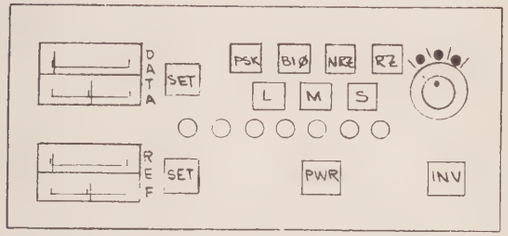
REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B					

J805 - MS-3102A - 16S - 1P
MATE - MS-3106B - 16S - 1S
POWER - D & E
CIRCUIT GRD - G
CHASSIS GRD - A

TOP



VIEW B

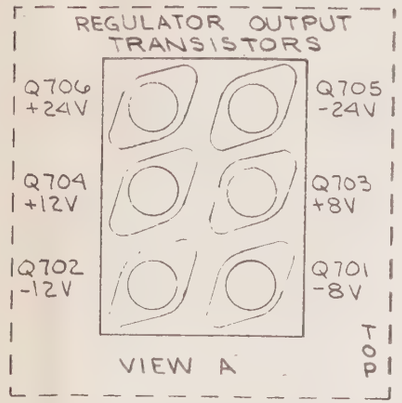


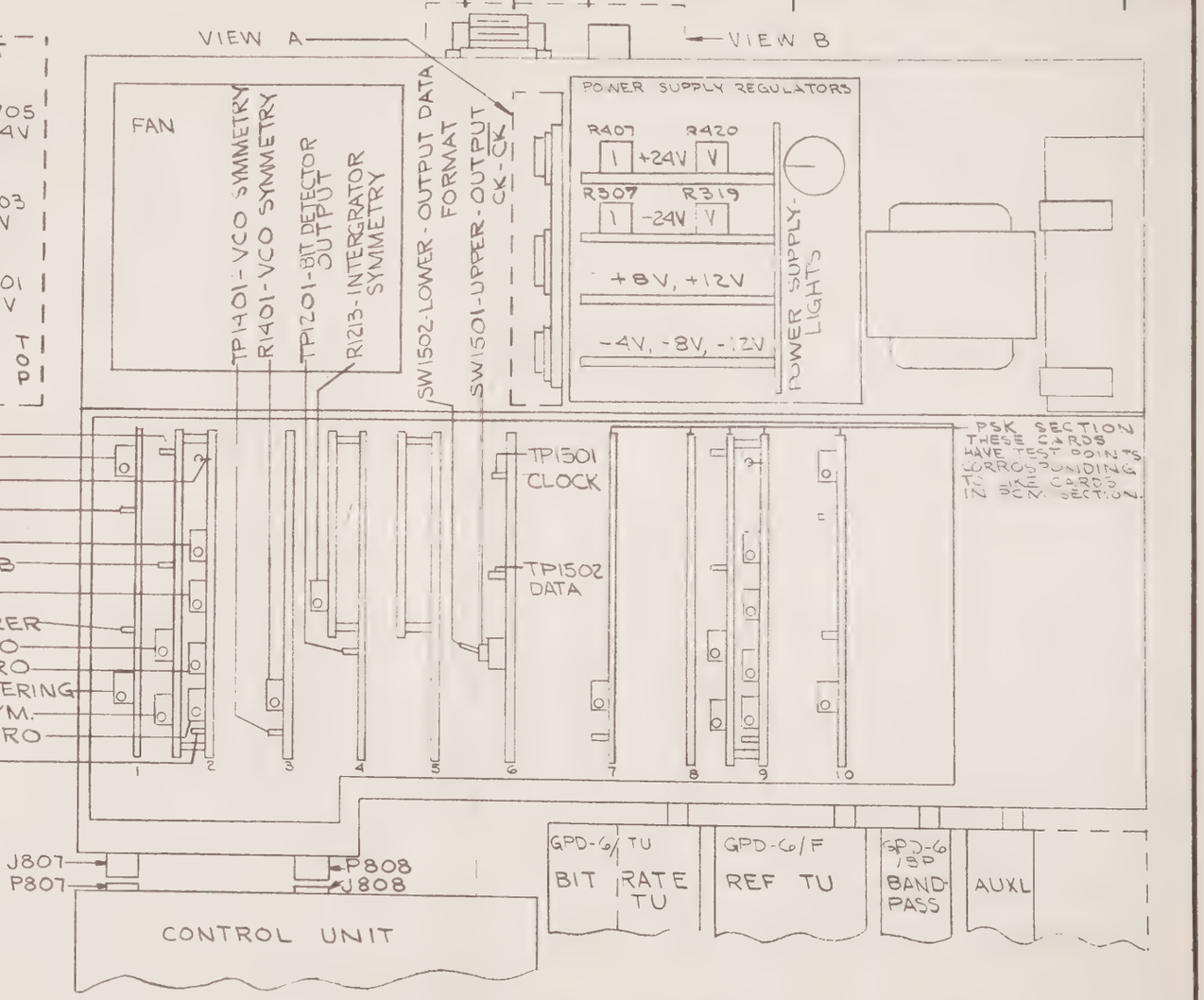
CONTROL UNIT PANEL

BOARD SERIES

PCM
- 1.) — 1000 — DC RESTORER
- 2.) — 1100 — VCO - LOWER BD.
  — 1700 — PHASE COMPARATOR
- 3.) — 1400 — METER
- 4.) — 1200 — BIT DETECTOR
- 5.) — 1300 — RZ CODE CONVERTER - LOWER
  — 1600 — RZ CODE CONVERTER - UPPER
- 6.) — 1500 — NRZ CODE CONVERTER - LINE DRIVERS

PSK
- 7.) — 1400 — METER
- 8.) — 1800 — SYNCHRONOUS DETECTOR - LINE DRIVER
- 9.) — 1100 — VCO - LOWER BD.
  — 1700 — PHASE COMPARATOR
- 10.) — 1000 — DC RESTORER





ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY./ASSY.

REF.	DESCRIPTION	QTY

GPD-6		
PRODUCT	NEXT ASSEMBLY	QTY./ASSY.

DATA CONTROL SYSTEMS, INC.

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ⌒ /IN.
FRACTIONAL HOLES ⌀.0, + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ✓

DWN.	J.E. HOLZE	DATE 4/17/-8
CHKD.		4/17/-8
ENG.		4/17/-8
APP.		4/68
SCALE		

DO NOT SCALE DRAWING

TITLE
CARD AND TEST POINT LOCATIONS
GPD-6

Figure 5-3. Card Locations, Test Points & Controls

BT -017756 REV. A

SHEET

5-6. PREVENTIVE MAINTENANCE.

5-7. VISUAL INSPECTION. Remove the cover by loosening all screws. Check all circuit boards for component damage, oxidized surfaces, burned resistors and also pins for proper alignment and good connection. Also check all connector jacks for good connection. Check complete chassis for dirt and dust between circuit boards and bottom chassis.

5-8. CLEANING. Because cooling air is constantly flowing through the equipment, the blower should be properly filtered. All corners and bottom of chassis should be cleaned periodically with a standard vacuum cleaner. All interior parts must be cleaned by air jet. The front panel and covers of the GPD-6 may be cleaned with carbon met or any suitable solvent.

5-9. BLOWER LUBRICATION. If the GPD-6 is used in temperatures exceeding 110°F or under severe vibration conditions, the fan should be lubricated at least once a year with a good grade lubricant.

5-10. PERIODIC CALIBRATION.

5-11. It is recommended that this series of adjustments be made every 3 to 6 months, depending on usage and severity of operating conditions. Dependable and accurate performance of the GPD-6 will thus be assured. Refer to Figures 5-1, 5-2, and 5-3, and Section VI drawings.

5-12. Do not operate the GPD-6 unless the fan cover is on to direct cooling air to the power transistors.

5-13. POWER SUPPLIES:

Calibration: P. C. Boards 100, 200, 300, 400 and 500

Test Equipment VTVM: 16 ohm 500 watt resistor
9 ohm 75 watt resistor
24 ohm 50 watt resistor
8 ohm 75 watt resistor

Test Procedure:

a. Remove all circuit boards except the 5 power supply boards located at the rear of the GPD-6.

b. Turn the power ON by depressing the power button on the front panel.

c. Insert a digital voltmeter across the -24 volt terminal and ground, use no load. Adjust R319 voltage adjust potentiometer on -24 volt power card #300 so that the voltage is exactly -24 volts.

d. With the same digital voltmeter, measure the voltage across the +24 volt terminal and ground. Adjust R420 voltage adjust potentiometer on power card #400 so that this voltage is exactly +24 volts.

e. Repeat step c. If -24 volts reading has changed, repeat step d. With the voltmeter across the -24 terminals and ground, momentarily short these terminals with a jumper. The voltage should remain at ground due to the short-circuit protection power cutoff of the GPD-6.

f. Switch the unit OFF then ON after wait, and repeat the shorting procedure to the +24 voltage terminal and ground.

g. Load the -24 volt supply with a ±6 ohm, 50 watt resistor to ground, and adjust R308 current adjust potentiometer on power card #300 to a voltage just beyond the point where further adjustment would begin to lower the -24 voltage.

h. With the 16 ohm resistor still loading the -24 volt supply, connect the voltmeter and a 24 ohm 50 watt resistor across the +24 volt terminal and ground. Adjust R407 current adjust potentiometer on power card #400 until further adjustment would lower the +24 volts. Remove both resistors from the -24 and +24 voltage terminals and ground.

i. Momentarily load the -24 volt supply with a 9 ohm 75 watt resistor. This should cause the voltage to drop to -20 volts ±1 volt. Repeat, using a 6 ohm, 75 watt resistor and the voltage should drop to ground. Remove the resistor and turn the power off. Wait 10 seconds, then turn the power on again.

j. Momentarily load the +24 Volt supply with an 8 ohm 75 watt resistor. The voltage should drop to +20 volts ±1 volt. Repeat using a 6 ohm 75 watt resistor. The voltage should now drop to ground. Remove resistor, turn power off and wait 10 seconds. Then turn the power on again.

k. Check the ±8 and ±12 volt supplies: these should be maintained within ±2.5% of their rated voltages. The ±8 supplies can range from ±7.8 to ±8.2 volts. The ±12 volt supplies can range from ±11.7 to ±12.3 volts. The -4 volt supply should range between -4 and -5 volts.

5-14. DATA LOOP CALIBRATION. The following separate setups and adjustments calibrate the d.c. restorer, limiter, phase-locked loop, integrator and bit detector and Data Loop frequency meter.

5-15. The square wave generator, used for simulating data in the following tests, corresponds in frequency to 1/2 the actual bit rate marked on the Tuning Unit. In NRZ code the data bit rate equals the bit rate marked on the tuning unit, but the maximum data rate (square wave) is only 1/2 the bit rate marked on the Tuning Unit.

5-16. DC RESTORER, LIMITER AND DOUBLER: P. C., Boards 1000 and 1700.

a. Setup

Test Equipment:	Scope Square Wave Generator GPD-6 Tuning Unit 16 - 25 kbs
Input Conditions:	10.25KHz square wave NRZ Code

b. Test Procedure

1. Place square wave generator output on rear input connector J801. Ground scope probe A and center the trace line on the .05 volt/cm D. C. range. Use X10 probe.
2. Put scope probe A on test point 1001 and observe for an undistorted square wave.
3. Ground the input and sweep the limiter center pot R1016 from one end to the other, noting any discontinuities. Set R1016 for 0 volts at test point 1001 on the .05 volt/cm scope range.
4. Reconnect signal input. Put scope probe A on test point 1002. The square wave should be between 1.5 and 2.5 volts peak-to-peak referenced at -12 volts.
5. Place scope probe A on test point 1702. Adjust the scope sweep to display one full cycle of this square wave for 10 cm. Adjust data symmetry pot R1039 for a 50% duty cycle with the 180° point at the center of trace.
6. With scope probe A on test point 1702 place scope probe B on test point 1002, or on the front panel IN terminal. The square wave on the A trace will be twice the frequency of the B trace.

5-17. PHASE LOCK LOOP. Adjustments for the Phase Comparator, DC Amplifier, VCO and Frequency Control Buss Voltage. P. C. Boards 1100 and 1700.

a. Setup

Test Equipment	Square Wave Generator Scope VTVM Frequency Counter GPD-6 Tuning Unit 16 - 25 kbs
Input Conditions:	10.25KHz square wave NRZ-L Code Format
Output Code:	RZ

b. Test Procedure

1. The zero VTVM on the 1.5 volt d-c scale. Adjust the GPD-6/TU pot five turns from either end (center frequency). Depress SET pushbutton of Data Loop.
2. Place the VTVM d-c probe on test point 1701 and adjust zero adjust pot R1139 for 0 volts on the VTVM 1.5 vdc scale.
3. Ground the square wave generator input. Leave the VTVM on test point 1701. Release SET Pushbutton and adjust phase comparator zero pot R1149 for 0 volts on the VTVM. The response to this adjustment is slow.
4. Depress Data Loop SET Pushbutton. Place the scope probe A on VCO board #1100 at the junction labeled "CR1107 VCO", in Figure 5-3, found at the inside left corner of the circuit board. The waveshape observed should be triangular, approximately 5.5 volts peak-to-peak.
5. Connect the frequency counter to the Vertical Out terminal of the scope. Adjust the VCO frequency pot R1105 until 20.5KHz is read on the frequency counter.
6. Place scope probe A on the CLOCK out jack and flip the RZ-NRZ output switch to the RZ position (right). The RZ code CLOCK should be the same frequency as the VCO, 20.5KHz.
7. Set the scope on and set the sweep rate to display one full CLOCK cycle for 10 cm by adjusting the scope time base and variable pot. Adjust VCO symmetry pot R1115 for a 50% duty cycle with the 180° point at the center of the trace. Make sure that the positive and negative trace portions are equal. If necessary, readjust the VCO frequency pot R1105 to read 20.5KHz on the counter.

8. Remove the input ground, and reinsert the square wave generator into the rear input connector. Place scope probe A on the terminal marked CR1107-VCO, and trigger the scope externally with the square wave generator signal. Release SET pushbutton. Place the VTVM probe on test point 1101, and sweep the input frequency from 8.2KHz to 12.3KHz. If the GPD-6 remains locked on the input signal the triangular VCO wave on the scope should remain stationary, and the VTVM should vary from -2.5 volts to +2.5 volts while sweeping the input frequency. If the triangular VCO signal should jump rapidly or appear to slip, it is an indication of a loss of lock on the input square wave signal.

5-18. QUADRATURE VCO SYMMETRY ADJUSTMENT. P. C. Boards 1100 and 1700.

a. Setup

Test Equipment:	Scope Noise Generator (specially balanced) GPD-6 Tuning Unit 16 - 25 kbs
Input Conditions:	2 volts RMS noise NRZ-L Format

b. Test Procedure

1. Place the VTVM on test point 1701. The reading should be 0 volts. If not, adjust frequency control buss amp zero pot R1139 for 0 volts.
2. Set the noise generator range switch in the RF position and adjust the output for 2 volts rms.
3. Put the noise generator output in the rear input connector, J801. The voltage at test point 1701 should be 0 ±.3 volts. If not, adjust the VCO Quadrature Symmetry pot R1735 for a reading of 0 ±.3 volts at test point 1701.

5-19. INTEGRATOR AND BIT DETECTOR ADJUSTMENT. P. C. Board 1200.

a. Setup

Test Equipment:	Square Wave Generator Scope GPD-6 Tuning Unit 16 - 25 kbs
Input Conditions:	10.25 square wave NRZ code

b. Test Procedure

1. Place scope probe A on the INT front panel jack.

2. To check for normal operation of the Integrator under locked conditions, trigger the scope externally with the triangular voltage at "CR1107 VCO". The integrations should appear as alternate positive and negative sawtooths, symmetric about the base line. If integration not symmetric, adjust R1201 for symmetry. Adjust the square wave generator for 5.12KHz, and note that the integrations now appear as alternately 2 positive and 2 negative sawtooths in the same triggering period. Note also that the height of these sawtooths has not changed from that of the single integrations.

3. Proper bit rate tracking under locked conditions may be checked by depressing the Data Loop SET Pushbutton and varying the square wave generator frequency ±20% from 10.25KHz. The pattern on the scope should now show simultaneous (+) and (-) integrations (sawtooths) at both frequency extremes, indicating no lock. Now release the SET Pushbutton at these frequency extremes noting that normal, alternate (+) and (-) integrations reappear indicating that the Integrator is tracking properly.

4. Put scope probe A on test point 1201, Bit Detector output. Place scope probe B on the IN terminal. Observe the two square waves 180° out of phase.

5. Press the INVert button. The two square waves should now be in phase.

5-20. METER CIRCUIT ADJUSTMENT. P.C. Board 1400.

a. Setup

Test Equipment:	Square Wave Generator VTVM Scope GPD-6 Tuning Unit 16 - 25 kbs
Input Conditions:	10.25KHz square wave NRZ code

b. Test Procedure

1. Put scope probe A on test point 1401 and depress the SET Pushbutton. Internal scope trigger. The observed pattern is the meter balance output.

2. Adjust the scope sweep to display one full cycle of this pattern for 10 cm. Adjust VCO symmetry pot 1401 for a 50% duty cycle with the 180° point at the center of trace.

3. Trigger the scope externally with the input square wave. Check the meter deflection by sweeping the input frequency back and forth. The meter should deflect full scale to 10 when the input frequency approaches the VCO frequency. The meter will register the beats between the two frequencies as the difference approaches zero. The beats should also be observed at the INTEG front panel terminal. Releasing the SET Pushbutton when meter is at maximum should cause the internal VCO to "lock" with the external signal.

5-21. REFERENCE LOOP CALIBRATION. The procedure for calibrating the d.c. restorer, limiter, phase-locked loop and meter is exactly the same as the Data Loop calibration procedure above. The printed circuit boards are identically numbered as the Data Loop, but located as a group to the right of the Data Loop boards. Follow each procedure in paragraphs 5-15 to 5-20 and use the GPD-6/F 8 to 12.5KHz plug-in unit instead of the GPD-6/TU.

5-22. There are no adjustments to make in the synchronous detector and reset function. However, the entire Reference Loop may be checked out following the Performance Test of paragraph 5-29.

5-23. PERFORMANCE TESTS.

5-24. These performance tests check the Reference Loop, output DATA and CLOCK synchronization and agreement, all code converters and the overall Model GPD-6 performance accuracy and synchronization.

5-25. It is assumed that the Model GPD-6 has been properly calibrated before these performance tests are attempted.

5-26. DATA AND CLOCK SYNCHRONIZATION TESTS. P.C. Boards 1500 and 1600.

a. Setup

Test Equipment:	Square Wave Generator Scope GPD-6 Tuning Unit 16 - 25 kbs
Input Conditions:	Square Wave: NRZ-L - 10.25KHz RZ - 10.25KHz
Output Conditions:	RZ = CLOCK NRZ = CLOCK/2

b. Test Procedure

1. Place square wave generator at the input connector. Place scope probe A on DATA terminal, and scope probe B on CLOCK terminal.
2. Test the CLOCK and DATA relationship for RZ code output by flipping the RZ-NRZ switch to the RZ position. Adjust the square wave generator for 10.25KHz and select RZ input format. Observe the square wave on both traces for CLOCK and DATA. Both traces should be at the same frequency. Set input for NRZ-L format. The CLOCK should now be equal to twice data frequency of 20.5KHz.
3. Test CLOCK and DATA relationship for NRZ-L code output by flipping the RZ-NRZ switch to the NRZ position. Adjust the square wave generator for a 10.25KHz and set for NRZ-L input format. Observe the square wave on both traces: the DATA frequency should be 1/2 the CLOCK frequency. Set for RZ input format. The DATA frequency should be 1/2 the CLOCK frequency.

5-27. CODE CONVERTER TESTS. These test require use of a variable 16 bit digital word generator to check the action of all logic elements in the Code Converter. Figure 5-4, Code Converter Timing Diagram, shows the action of each element when converting a special artificial 8 bit work to RZ code.

Boards: 1300 1600 and 1500

5-28. This artificial 8 bit word is generated by using a 16-bit NRZ word to control each half-bit of an eight-bit word. The resulting eight-bit word has deliberate errors for test purposes.

a. Setup

Test Equipment:	GPD-6 Tuning Unit 16 - 25 kbs 16 bit variable word generator Scope
Input Conditions:	See Text

b. Test Procedure

1. Place digital word generator cable on input connector J801. Place scope probe A on the IN terminal and scope probe B on test point 1602.

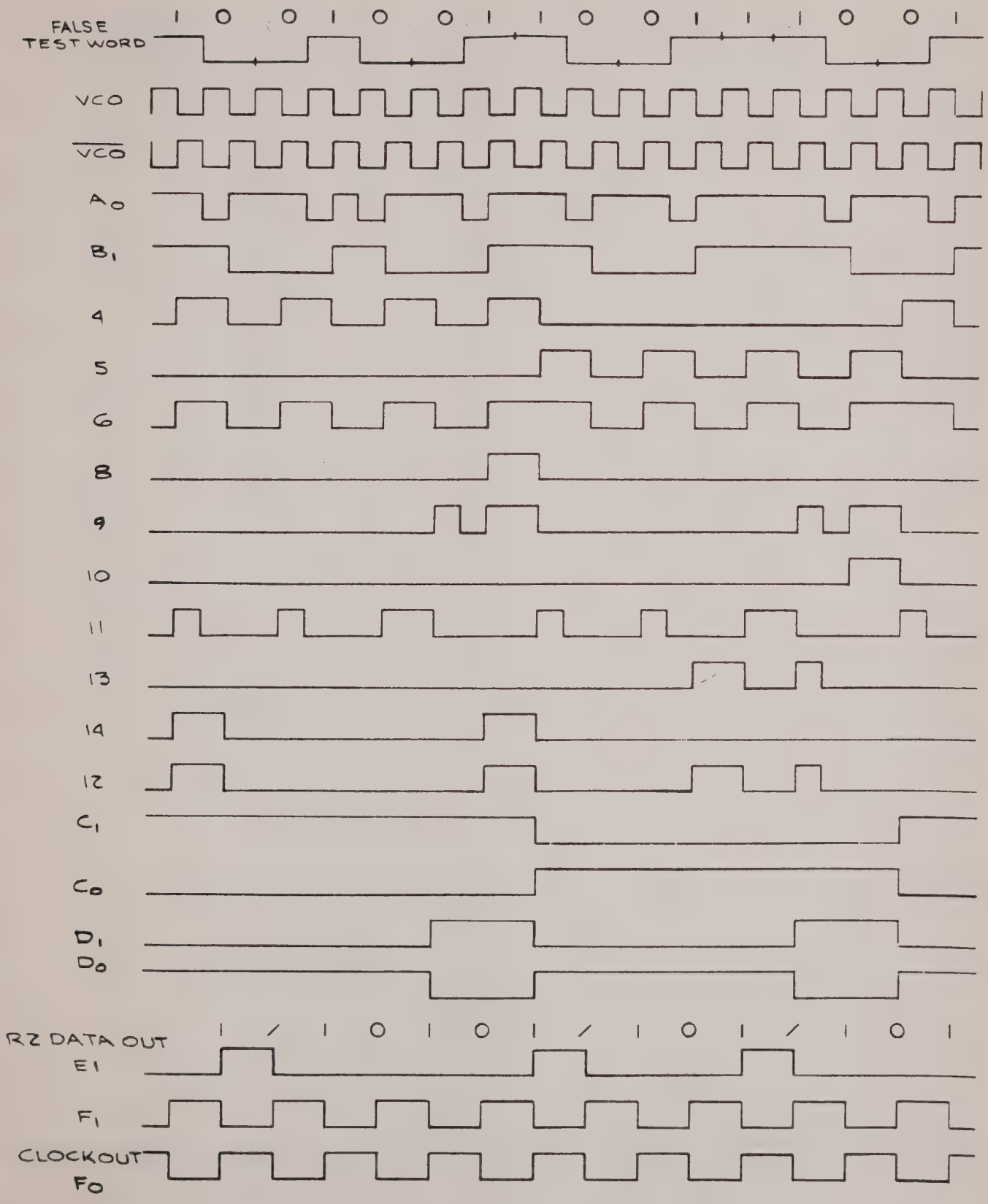


Figure 5-4. Code Converter Timing Diagram

2. Set the sixteen bit word generator in the NRZ-L format position. Place bit switches in alternate 1 and 0 positions: 1010101010101010. Adjust the resulting square wave to 10.25KHz. This square wave now represents consecutive, 8-bit RZ words: each half bit is controlled by a separate switch.

16 switch positions	10	10	10	10	10	10	10	10
8-bit RZ word	1	1	1	1	1	1	1	1

3. Lock the Data Loop to the input frequency (see para. 3-15). If necessary, adjust GPD-6/TU screw pot. Set the format/mode switch to NRZ-M.

4. Set RZ-NRZ output switch to RZ position. Without changing generator frequency, change generator bit switches to the following positions 1001001100111001. This is a false 8-bit word used to check the error correcting features of the Code Converter. The resulting 8-bit RZ word at test point 1602 should be either (1) 10011010 or (2) 10010100.

5. The timing diagram (Figure 5-4) indicates the conditions of the various gates and flip-flops when the false word is being generated. Either word is the only correct output at test point 1602.

6. The DATA out at DATA front panel jack will be the following RZ word: 101101010100101.

7. Check NRZ, RZ, using random 16-bit words after properly locking on data.

8. The preceding tests are conclusive that the code converter is operating correctly.

5-29. OVERALL PERFORMANCE TESTS. (Parts I and II)

a. Part I Procedure - Reference Loop Demodulation.

1. Test Equipment: 16-Bit Variable Word Generator
Dual-Trace Scope
GPD-6/TU 16 to 25 kbs
GPD-6/F 8 to 12.5 KHz

2. Input Conditions: (see Figure 5-5) Bi-Phase-L 8-bit word: 10100110 @ 10.25KHz

3. Output Conditions: (see Figure 5-5) NRZ-L or $\overline{\text{NRZ-L}}$ at DET front panel jack

4. Test Procedure Part I

a. Apply power to Model GPD-6 and test equipment.

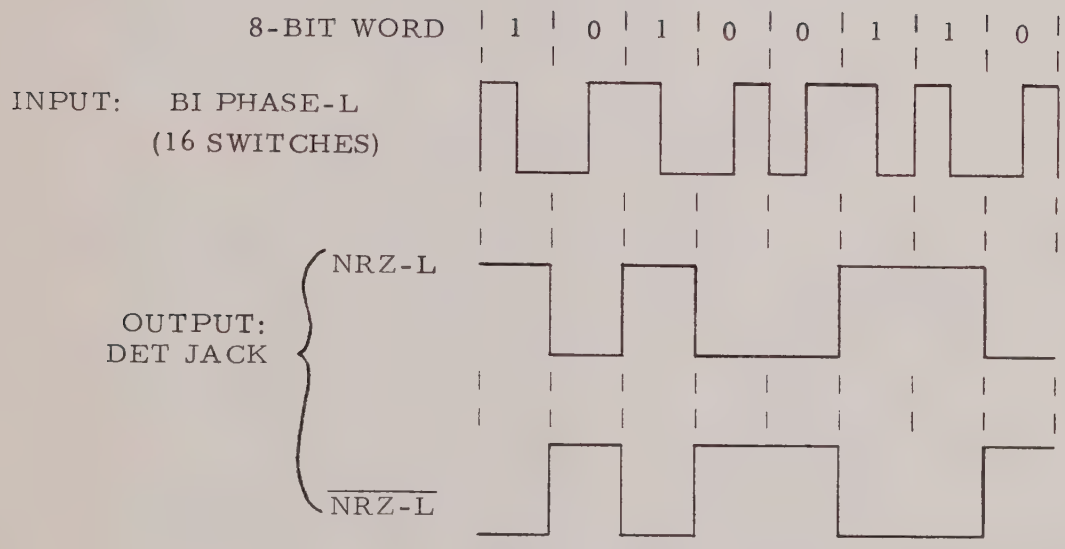


Figure 5-5. BIØ-L Demodulation in Reference Loop

b. Set Variable Word Generator Bi-Phase-L format. Set switches to alternate "1"s and "0"s (1010101010101010) and set output frequency to 10.25KHz. Connect generator to rear input connector J801.

c. Set Format/Mode Switch on GPD-6 to Bi-Phase-L position.

d. Lock Reference Loop VCO to generator frequency as specified in paragraph 3-14 of Operation Section.

e. Lock Data Loop VCO to Reference Loop output according to paragraph 3-15 of Operation Section.

f. Apply scope probe A to generator output: apply scope probe B to DET jack. Line up A and B traces.

g. Set generator switches as follows (1001100101101001) to obtain the Bi-Phase-L 8-bit word.

h. Check lower scope trace for exact correspondence to Figure 5-5 showing the Bi-Phase-L input word and either NRZ-L or $\overline{\text{NRZ-L}}$ conversion.

i. Maintain setup and equipment for Part II.

b. Part II Procedure - Combined Reference and Data Loop Performance.

1. Test Equipment: Same as Part I
2. Input Conditions: Same as Part I
3. Output Conditions: Various. Perform test.
4. Test Procedure Part II

a. All equipment and input conditions are the same as Part I.

b. Place scope probe B on DATA front panel jack.

c. Place Format/Mode Switch in PSK-NRZ-L position.

d. Place NRZ-RZ output DATA switch in NRZ position.

e. Open and close Reference Loop by depressing and releasing the REF SET pushbutton. The output waveform on scope probe B should alternate from DATA to $\overline{\text{DATA}}$ as the SET pushbutton is alternately depressed and released.

f. Place Format/Mode Switch in Bi-Phase-L position.

g. The output waveform on scope probe B should remain DATA when the REF SET pushbutton is alternately depressed and released. This test establishes that the synchronous detector reset function is operating normally.

h. The NRZ-L output DATA should correspond exactly to the results obtained in Part I from the DET jack. Refer to Figure 5-5.

i. Place NRZ-RZ output DATA switch in RZ position and repeat previous steps (c) through (g). Check RZ output DATA for proper conversion from NRZ-L. See Figure 5-5.

5-30. TROUBLESHOOTING.

5-31. The Model GPD-6 will track PSK-NRZ, Bi-Phase carrier and PCM DATA signals accompanied by noise and accurately reconstruct the DATA bits. However, excessive noise can cause a temporary lose of lock on the signal. As soon as more normal conditions prevail, the Model GPS-6 will again lock on the signal to yield valid DATA and synchronous CLOCK.

5-32. Troubleshooting procedures are listed and contained in four troubleshooting charts. The procedures are grouped into the following malfunction categories: (I) Loop won't lock, (II) No output CLOCK, (III) No output DATA, and (IV) Erroneous output DATA. A look at the preliminary troubleshooting check list, in the next paragraph, before consulting the troubleshooting charts may save a great deal of wasted effort, especially if the malfunction is due to an oversight, operator's error or malfunctioning d. c. power supply.

5-33. PRELIMINARY TROUBLESHOOTING CHECK LIST.

a. Check that green power lamp is lit.

b. Check for correct GPD-6/TU and GPD-6/F modules for incoming frequency and bit rate.

c. Check Reference and Data loops for lock-on to frequency and bit rate. Observe upper meter in each loop.

d. Check Format/Mode Switch for correct setting to input DATA.

e. Check output DATA and CLOCK toggle switches for correct correspondence to desired output DATA format (see Table 3-2).

f. Make certain that the operating procedures of Section III are being followed as specified.

g. Check the -4, -8, +8, -12, +12 d. c. voltages on main connector board. If necessary calibrate supplies as specified in paragraph 5-13, Calibration Procedure.

5-34. TROUBLESHOOTING CHARTS. Each chart contains a procedure flow sequence to perform rapid troubleshooting. Test equipment should be used as outlined in paragraphs 5-14 through 5-17. If desired, troubleshooting may be accomplished using the incoming DATA signal. In either method, the Troubleshooting Charts assume that the Model GPD-6 is in calibration and that a malfunction is due to a failure of a particular circuit or function. Also, the Troubleshooting Charts assume that recalibration would not correct the malfunction, and, therefore, the Troubleshooting Charts limit the malfunction to a particular circuit board which should be replaced. All circuit boards replaced should be returned to Data-Control Systems, Inc. for repair.

5-35. The Troubleshooting procedure Charts refer to board number which contain the following functions:

	Board No.	Function
non-separable	1000	DC Restorer, Limiter, 1/2 Doubler
non-separable	1100	VCO, DC Amplifier
non-separable	1200	Bit Detector/Integrator
non-separable	1300	RZ Code Converter (lower)
non-separable	1500	NRZ Code Converter/Line Drivers
non-separable	1600	RZ Code Converter (upper)
non-separable	1700	Phase Comparator/VCO Quadrature Amplifier/ 1/2 Doubler
	1800	Synchronous Detector/Carrier Line Driver

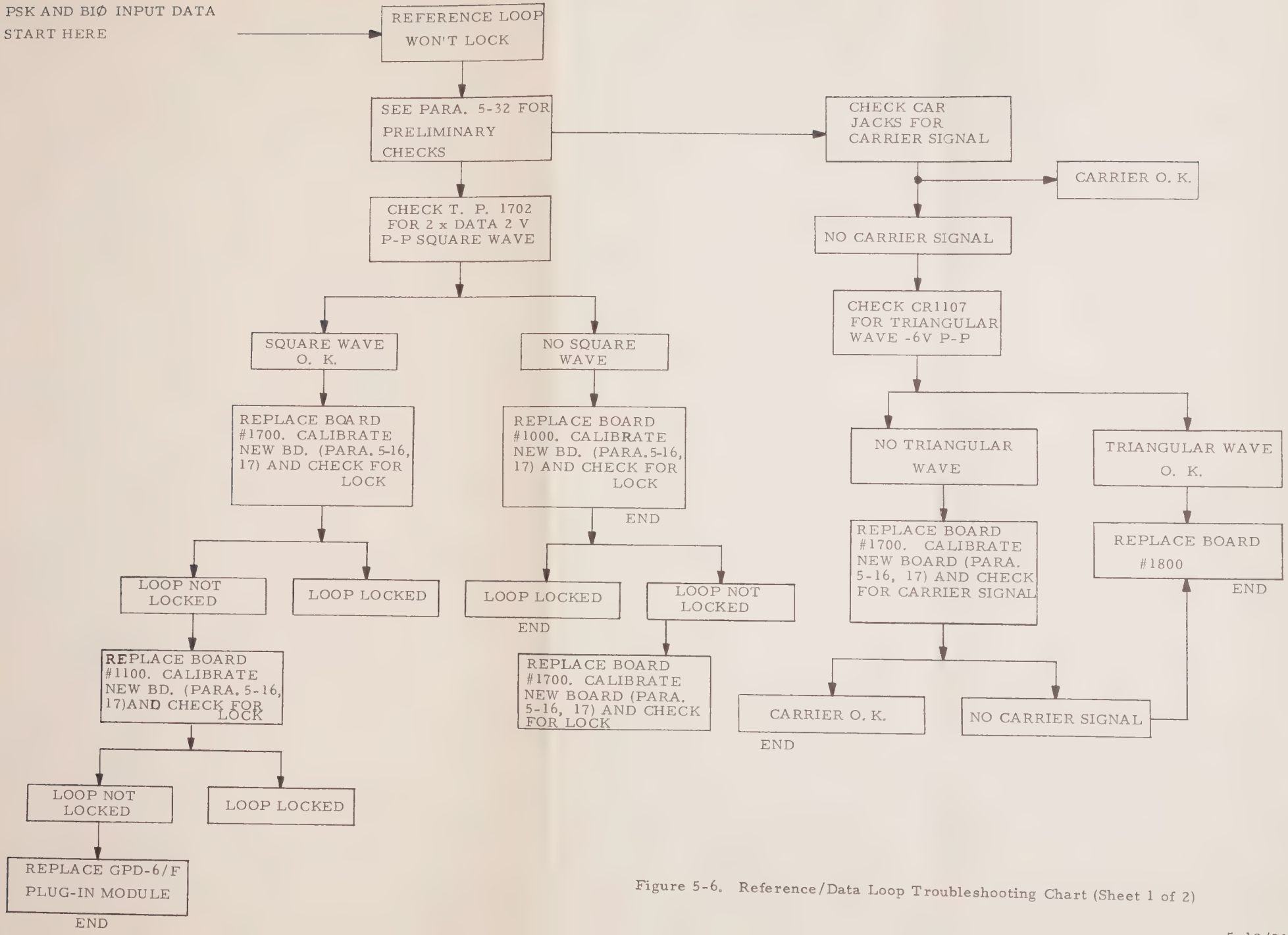

PSK AND BIØ INPUT DATA START HERE
REFERENCE LOOP WON'T LOCK
SEE PARA. 5-32 FOR PRELIMINARY CHECKS
CHECK T. P. 1702 FOR 2 x DATA 2 V P-P SQUARE WAVE
SQUARE WAVE O. K.
NO SQUARE WAVE
REPLACE BOARD #1700. CALIBRATE NEW BD. (PARA. 5-16, 17) AND CHECK FOR LOCK
REPLACE BOARD #1000. CALIBRATE NEW BD. (PARA. 5-16, 17) AND CHECK FOR LOCK
END
LOOP NOT LOCKED
LOOP LOCKED
LOOP LOCKED
END
LOOP NOT LOCKED
REPLACE BOARD #1100. CALIBRATE NEW BD. (PARA. 5-16, 17)AND CHECK FOR LOCK
REPLACE BOARD #1700. CALIBRATE NEW BOARD (PARA. 5-16, 17) AND CHECK FOR LOCK
LOOP NOT LOCKED
LOOP LOCKED
REPLACE GPD-6/F PLUG-IN MODULE
END
CHECK CAR JACKS FOR CARRIER SIGNAL
CARRIER O. K.
NO CARRIER SIGNAL
CHECK CR1107 FOR TRIANGULAR WAVE -6V P-P
NO TRIANGULAR WAVE
TRIANGULAR WAVE O. K.
REPLACE BOARD #1700. CALIBRATE NEW BOARD (PARA. 5-16, 17) AND CHECK FOR CARRIER SIGNAL
REPLACE BOARD #1800
END
CARRIER O. K.
NO CARRIER SIGNAL
END

Figure 5-6. Reference/Data Loop Troubleshooting Chart (Sheet 1 of 2)

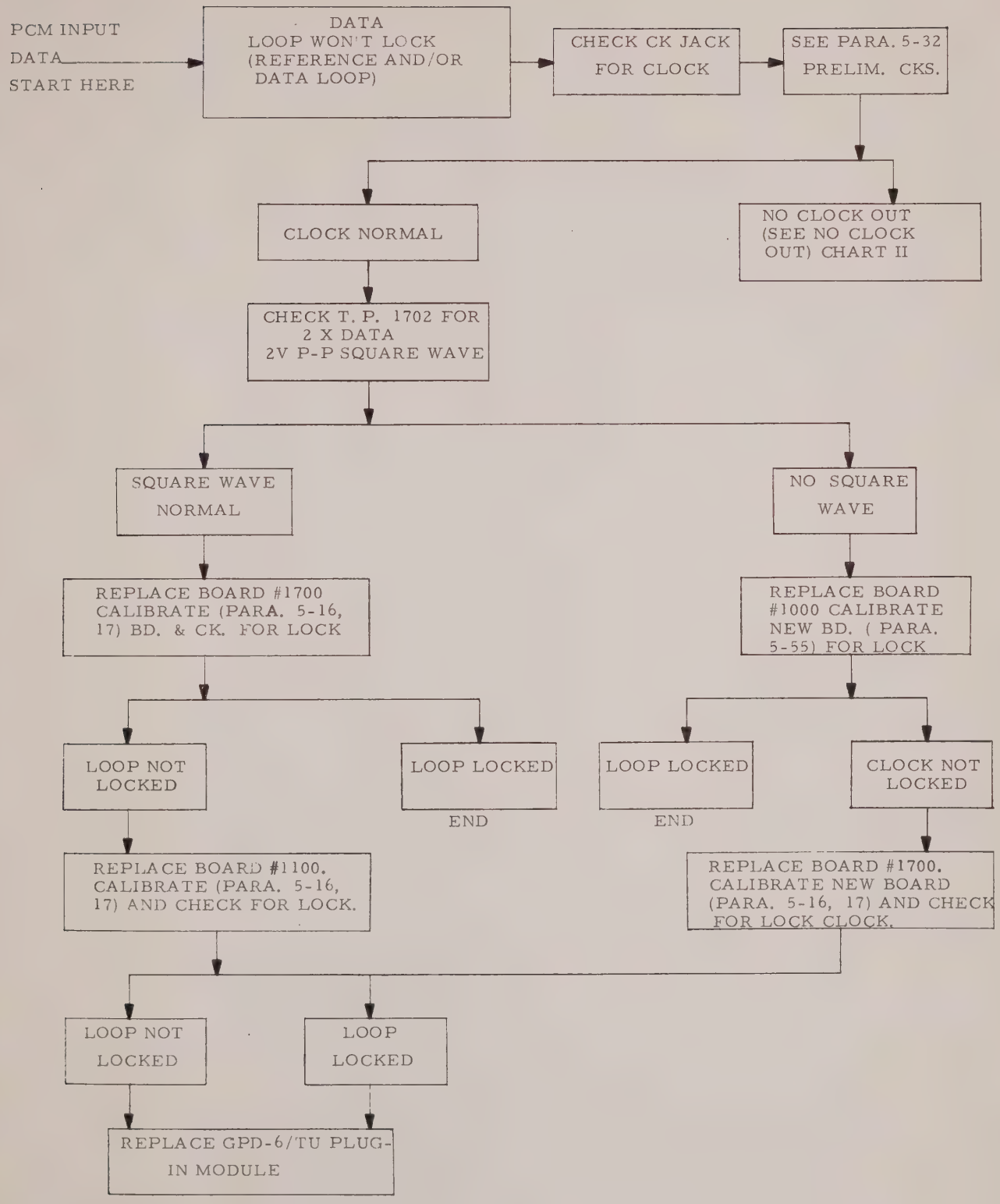

PCM INPUT DATA START HERE
DATA LOOP WON'T LOCK (REFERENCE AND/OR DATA LOOP)
CHECK CK JACK FOR CLOCK
SEE PARA. 5-32 PRELIM. CKS.
CLOCK NORMAL
NO CLOCK OUT (SEE NO CLOCK OUT) CHART II
CHECK T. P. 1702 FOR 2 X DATA 2V P-P SQUARE WAVE
SQUARE WAVE NORMAL
NO SQUARE WAVE
REPLACE BOARD #1700 CALIBRATE (PARA. 5-16, 17) BD. & CK. FOR LOCK
REPLACE BOARD #1000 CALIBRATE NEW BD. (PARA. 5-55) FOR LOCK
LOOP NOT LOCKED
LOOP LOCKED
END
LOOP LOCKED
END
CLOCK NOT LOCKED
REPLACE BOARD #1100. CALIBRATE (PARA. 5-16, 17) AND CHECK FOR LOCK.
REPLACE BOARD #1700. CALIBRATE NEW BOARD (PARA. 5-16, 17) AND CHECK FOR LOCK CLOCK.
LOOP NOT LOCKED
LOOP LOCKED
REPLACE GPD-6/TU PLUG-IN MODULE

Figure 5-6. Reference/Data Loop Troubleshooting Chart (Sheet 2 of 2)

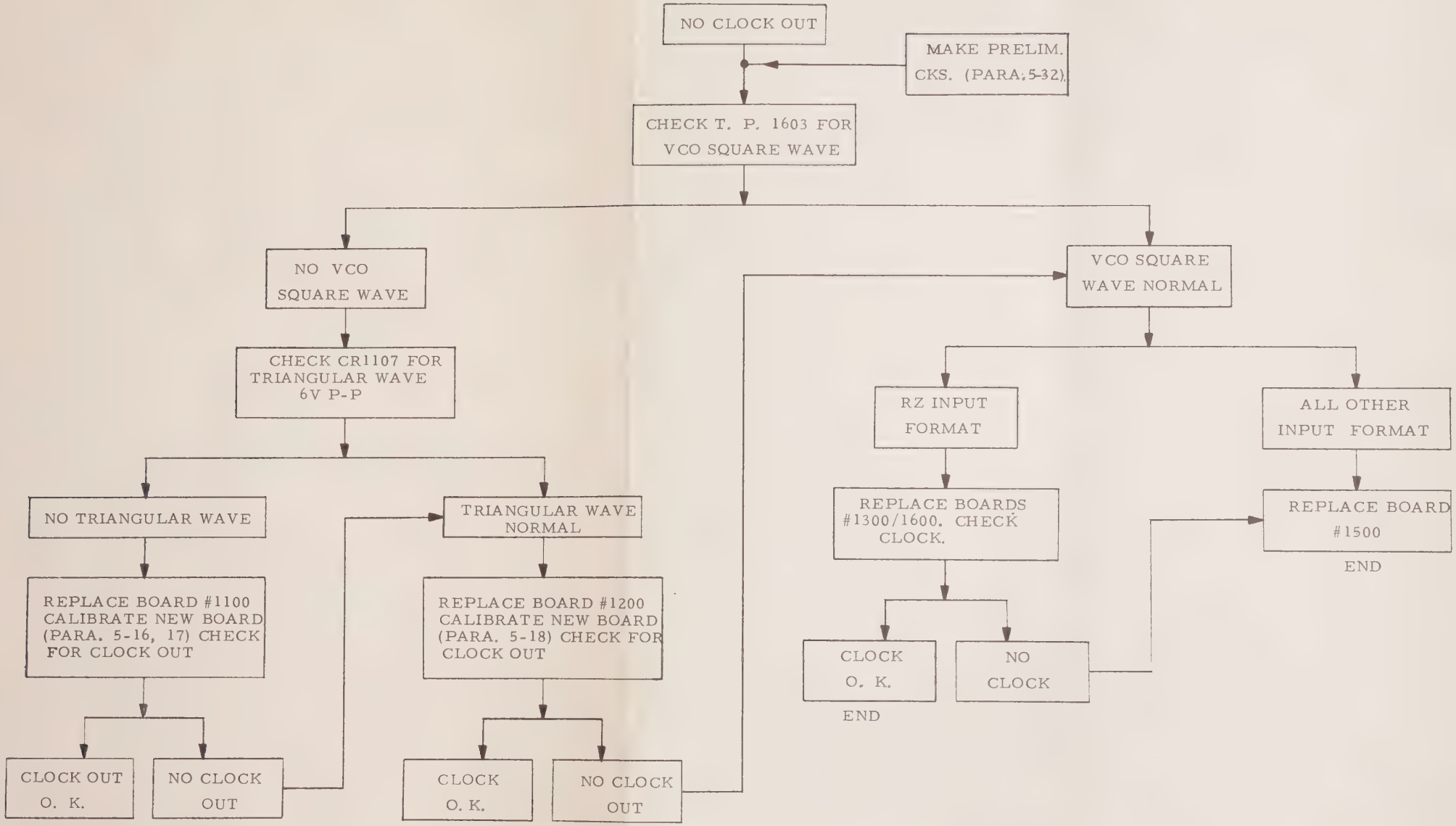

NO CLOCK OUT
MAKE PRELIM. CKS. (PARA. 5-32).
CHECK T. P. 1603 FOR VCO SQUARE WAVE
NO VCO SQUARE WAVE
CHECK CR1107 FOR TRIANGULAR WAVE 6V P-P
NO TRIANGULAR WAVE
REPLACE BOARD #1100 CALIBRATE NEW BOARD (PARA. 5-16, 17) CHECK FOR CLOCK OUT
CLOCK OUT O. K.
NO CLOCK OUT
TRIANGULAR WAVE NORMAL
REPLACE BOARD #1200 CALIBRATE NEW BOARD (PARA. 5-18) CHECK FOR CLOCK OUT
CLOCK O. K.
NO CLOCK OUT
VCO SQUARE WAVE NORMAL
RZ INPUT FORMAT
REPLACE BOARDS #1300/1600. CHECK CLOCK.
CLOCK O. K.
END
NO CLOCK
ALL OTHER INPUT FORMAT
REPLACE BOARD #1500
END

Figure 5-7. No Clock Troubleshooting Chart.

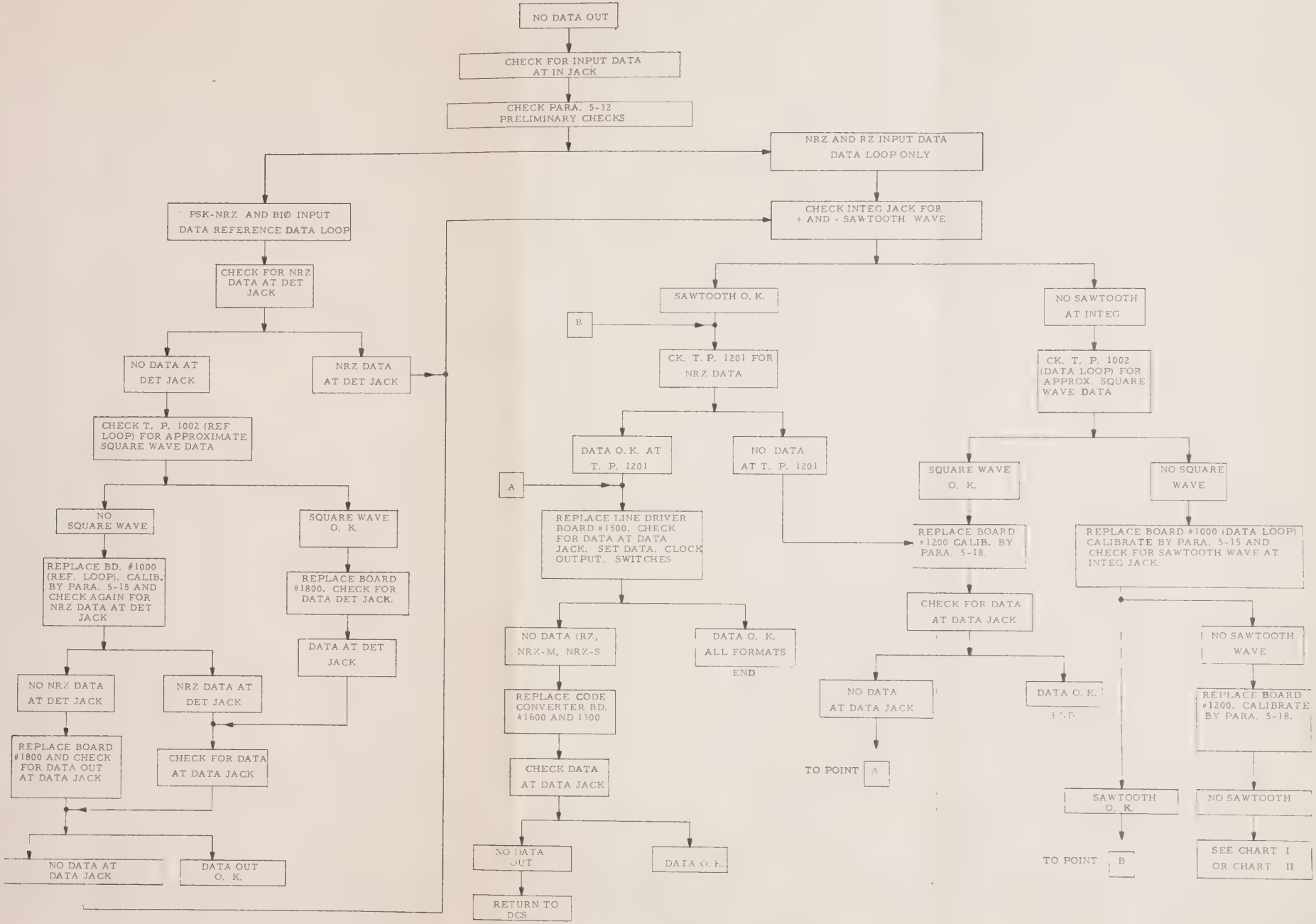
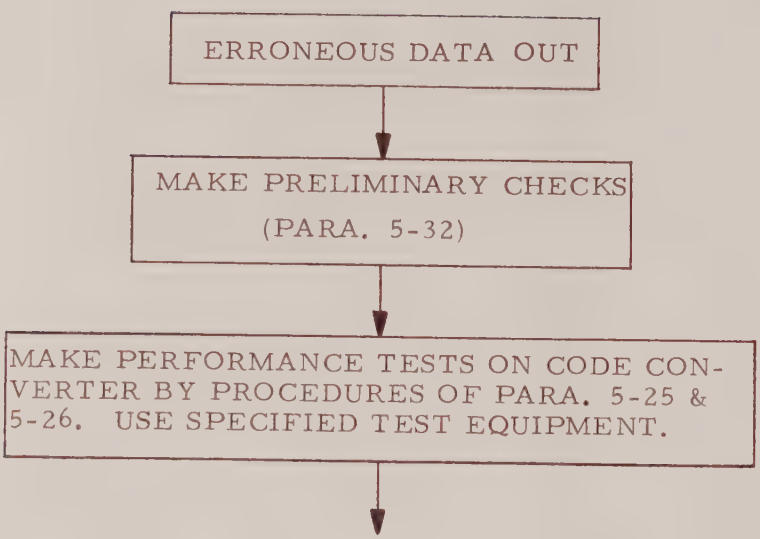

NO DATA OUT
CHECK FOR INPUT DATA AT IN JACK
CHECK PARA. 5-32 PRELIMINARY CHECKS
NRZ AND RZ INPUT DATA DATA LOOP ONLY
PSK-NRZ AND BIØ INPUT DATA REFERENCE DATA LOOP
CHECK INTEG JACK FOR + AND - SAWTOOTH WAVE
CHECK FOR NRZ DATA AT DET JACK
SAWTOOTH O. K.
NO SAWTOOTH AT INTEG
B
NO DATA AT DET JACK
NRZ DATA AT DET JACK
CK. T. P. 1201 FOR NRZ DATA
CK. T. P. 1002 (DATA LOOP) FOR APPROX. SQUARE WAVE DATA
CHECK T. P. 1002 (REF LOOP) FOR APPROXIMATE SQUARE WAVE DATA
DATA O. K. AT T. P. 1201
NO DATA AT T. P. 1201
SQUARE WAVE O. K.
NO SQUARE WAVE
A
NO SQUARE WAVE
SQUARE WAVE O. K.
REPLACE LINE DRIVER BOARD #1500. CHECK FOR DATA AT DATA JACK. SET DATA. CLOCK OUTPUT. SWITCHES
REPLACE BD. #1000 (REF. LOOP). CALIB. BY PARA. 5-15 AND CHECK AGAIN FOR NRZ DATA AT DET JACK
REPLACE BOARD #1800. CHECK FOR DATA DET JACK.
REPLACE BOARD #1200 CALIB. BY PARA. 5-18.
REPLACE BOARD #1000 (DATA LOOP) CALIBRATE BY PARA. 5-15 AND CHECK FOR SAWTOOTH WAVE AT INTEG JACK.
NO DATA (RZ, NRZ-M, NRZ-S
DATA O. K. ALL FORMATS
END
CHECK FOR DATA AT DATA JACK
NO NRZ DATA AT DET JACK
NRZ DATA AT DET JACK
DATA AT DET JACK
NO SAWTOOTH WAVE
NO DATA AT DATA JACK
DATA O. K.
REPLACE CODE CONVERTER BD. #1600 AND 1300
REPLACE BOARD #1800 AND CHECK FOR DATA OUT AT DATA JACK
CHECK FOR DATA AT DATA JACK
REPLACE BOARD #1200. CALIBRATE BY PARA. 5-18.
TO POINT A
CHECK DATA AT DATA JACK
SAWTOOTH O. K.
NO SAWTOOTH
NO DATA AT DATA JACK
DATA OUT O. K.
NO DATA OUT
DATA O. K.
TO POINT B
SEE CHART I OR CHART II
RETURN TO DCS

Figure 5-8. No Data Troubleshooting Chart.


ERRONEOUS DATA OUT
MAKE PRELIMINARY CHECKS
(PARA. 5-32)
MAKE PERFORMANCE TESTS ON CODE CONVERTER BY PROCEDURES OF PARA. 5-25 & 5-26. USE SPECIFIED TEST EQUIPMENT.

With false word generated, refer to Figure 5-4 and check each flip-flop (A, B, C, D, E, F) and gate (4 through 12) for conformance to Figure 5-4 waveform and timing sequence. If any gate or flip-flop output differs, replace boards 1300 and 1600 and check for correct data output signal. If gates or flip-flop outputs conform to Figure 5-4, replace the Line Driver Board #1500 and check for correct DATA out.

Figure 5-9. Erroneous DATA Troubleshooting Chart

TABLE 5-2.

RECOMMENDED SPARE PARTS LIST FOR GPD-6 PSK DEMOD-PCM SYNCHRONIZER

Item	Part Number	Location	Description	Qty. Per 1 Unit	Unit Price	Total
1	PA-046-021	Front Panel	Switch, Centralab, 40C series, Code Format Selector	1	$ 52.50	$ 52.50
2	1182L56G1	Front Panel	Switch, Pendar, "PWR"	1	19.80	19.80
3	1034L56W1/A	Front Panel	Switch, Pendar, "SET" #1 and "SET" #2	1	22.75	22.75
4	1122L56W1	Front Panel	Switch, Pendar "INV"	1	29.15	29.15
5	327	Front Panel	Bulb, G.E., PWR, SET #1, SET #2 "INV" switches, PSK, B10, NRZ, RZ, L, M, S indicators	5	1.05	5.25
6	15291	Front Panel	Meter, International, "SET" #1, "SET" #2	1	51.25	51.25
7	15290	Front Panel	Meter, International, Phase Error #1, Phase Error #2	1	59.90	59.90
8	M-860	P/S	Transformer, Magnetic Corporation power	1	59.00	59.00
9	539-2647-01	P/S	Capacitor, Sangamo, 2500 MFD @ 50V, C2001, C2002	1	6.00	6.00
10	MR-324-R	P/S	Rectifier, Motorola, CR2001-CR2004	2	1.75	3.50
11	2N3790	P/S	Transistor, Motorola, Q701-Q706	3	24.50	73.50
12	Venturi Type	P/S	Muffin Fan, Rotron	1	30.45	30.45
13	11471	P/S	Card, DCS, -4volt, -8volt and -12volt (1 ea.)	1	34.50	34.50
14	11460	P/S	Card, DCS, +8volt and +12volt (1 ea.)	1	26.40	26.40
15	11467	P/S	Card, DCS, -24volt (1 ea.)	1	77.90	77.90
16	11465	P/S	Card, DCS, +24volt (1 ea.)	1	96.20	96.20
17	15197	P/S	Card, DCS, Indicator, P/S Lights (1 ea.)	1	22.00	22.00
18	11773/	Main Chassis	Card Assembly, DCS, RZ Code Converter (1 ea.)	1	316.20	316.20
19	15322	Main Chas.	Card, DCS Meter Board (2 ea.)	1	134.00	134.00
20	15144	Main Chas.	Card, DCS NRZ Code Converter Line Drivers (1 ea.)	1	112.00	112.00

Table 5-2 cont.

GPD-6 Spares Parts List (Cont.)

Item	Part Number	Location	Description	Qty. Per 1 Unit	Unit Price	Total
21	15151	Main Chassis	Card, DCS, Synchor Detector (1 ea.)	1	$ 110.00	$ 110.00
22	14155B/ 15154B	Main Chassis	Card Assembly, DCS VCO Phase Comparator PSK/VCO Phase Comparator PCM (2 ea.)	1	495.95	495.95
23	15166B	Main Chassis	Card, DCS, DC Restorer PSK/DC Restorer PCM (2 ea.)	1	125.00	125.00
24	15708/	Main Chassis	Card Assembly, DCS Bit Detector (1 ea.)	1	245.00	245.00
25	3AG	P/S	Fuse, Littlefuse, 250V, 1.5 AMP. Fast Blo	5	.70	3.50
			Prices subject to change without notice.		TOTAL	$2,211.70

SECTION VI

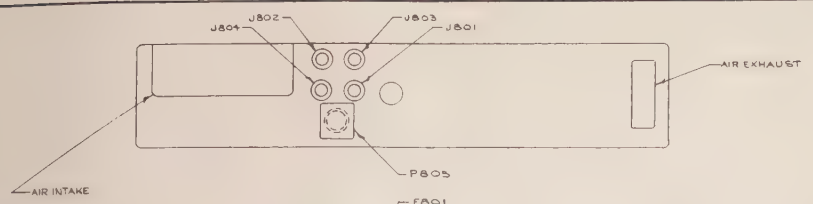
DRAWINGS

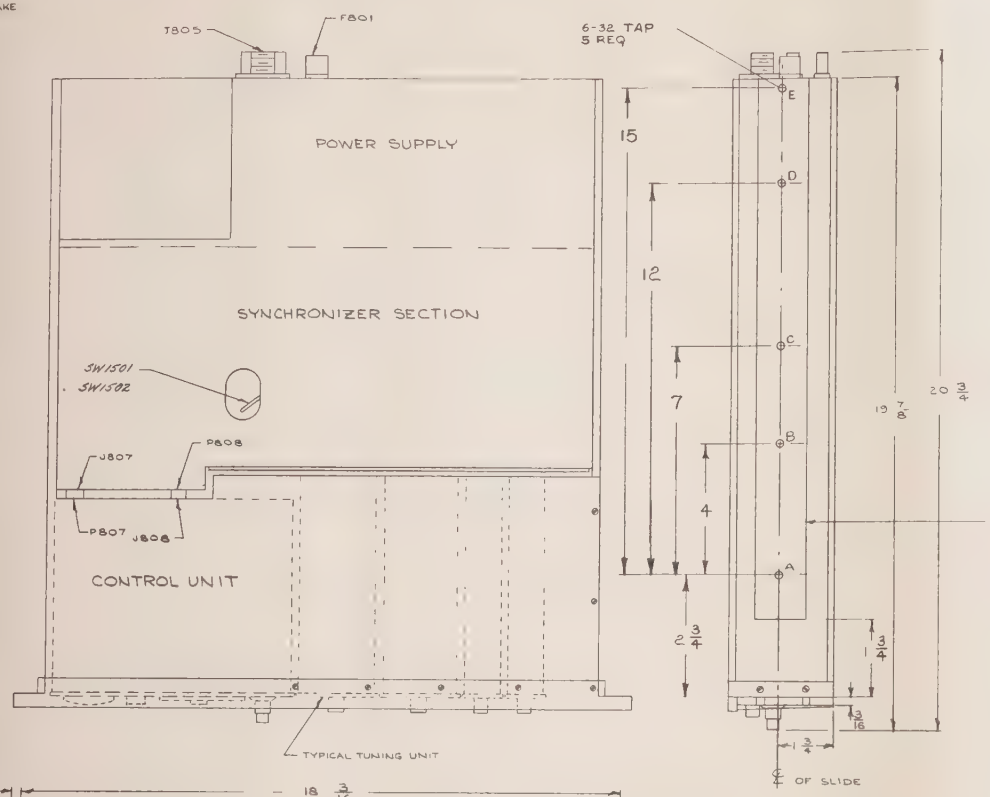
6-1. SCOPE.

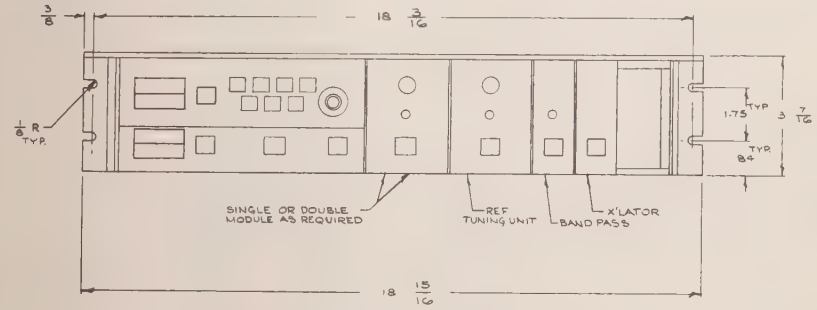
6-2. This section contains equipment assembly drawings, schematics, and block diagrams necessary for maintenance of the equipment.

DO-015272	Outline
GW-015532	Schematic DC Restorer
TW-015284	Schematic VCO Board
TW-015280	Schematic Comparator Board
RW-015283	Schematic Synchro Detector Board
TY-015731	Logic Diagram Code Converter
BD-015291	Meter Frequency Set
TW-016005	Wiring Schematic
TA-016003	Assembly Band Pass Filter (GPD-6/BP)
RA-017476	Board Assembly Band Pass Filter (GPD-6/BP)
GW-017475	Schematic Band Pass Filter (GPD-6/BP)
BB-015326	Block Diagram, Power Supply
BA-015276	Power Supply, Board Assembly-Mother
BA-011460	Power Supply, Board Assembly +8V +12V
BW-012745	Schematic Power Supply, +8V +12V
BA-011465	Power Supply, Board Assembly +24V
BW-012743	Power Supply, Schematic +24V
BA-011471	Power Supply, Board Assembly -4V -8V -12V
BW-012744	Schematic Power Supply -4V -8V -12V
BA-011467	Power Supply Board Assembly -24V
BW-012735	Schematic -24V Power Supply
BA-015197	Power Supply Board Assembly Indicator
BW-015277	Power Supply Schematic, Indicator
GA-015155	Phase Comparator Board Assembly
GA-015322	Meter Board Assembly
GW-015281	Meter Board Assembly Schematic
GA-015144	Board Assembly Data and Clock Line Drivers
GW-015282	Schematic, Line NRZ Code Converter Data and Clock Driver

GA-015151	Synchro Detector Board Assembly
TA-011773	Board Assembly Code Converter RZ (Lower)
TA-015708	Upper Board Assembly Bit Detector
TA-015709	Lower Board Assembly Bit Detector
GW-015624	Schematic Bit Detector Intergrating
DA-015186	Final Assembly Control Unit
BW-015297	Schematic Control Unit
TY-013026	Gate Location, Code Converter RZ (Lower)
DA-015271A	Final Assembly
GA-015166	DC Restorer Board Assembly
GA-015154	VCO Board Assembly
CA-012760	Final Assembly Double Mod Tuning Unit
CA-011173	Schematic-Double Mod. Tuning Unit
CW-012793	Schematic, Tuning Unit and Mother Board Term. Ident.
CA-015900	Final Assembly, GPD-6/F
CA-015301	Final Assembly Reference Tuning Unit, GPD-6/F
BW-017606	Schematic Data Quality, GPD-6/DQ
TA-017604	Board Assembly Data Quality, GPD-6/DQ
TA-015723	Assembly, Plug-In DC Restorer
CA-017557	Board Assembly Code Converter
BA-015185	Bracket Assembly Control Unit Lights
BW-015307	Schematic, GPD-6/F







REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	R & E REVISION. ADDED 6-32 SLIDE MTG HOLES	3/3/67	
~	C	CA-3678 ADDED NOTE #3	4/5/67	
—	D	CA-3982 CHGD, P805 TO J805 ON PICTORIAL VIEW	11/1/67	

NO	CONNECTOR	MATING CONNECTOR	NO	FUNCTION
J801	CONN, DAGE, UG-657/U	CONN, DAGE, UG-88C/U	P801	INPUT
J802	CONN, DAGE, UG-657/U	CONN, DAGE, UG-88C/U	P802	CLOCK OUT
J803	CONN, DAGE, UG-657/U	CONN, DAGE, UG-88C/U	P803	DATA OUT
J804	CONN, DAGE, UG-657/U	CONN, DAGE, UG-88C/U	P804	PSK CARRIER OUT
J805	CONN, MS3102A-16S-1P	CONN, MS3106B-16S-1S	P805	POWER
#4 J807	CONN, BURNDY, MS20RM-1	CONN, BURNDY, MS20PM-1	P807	
P808	CONN, AMP, 57-10360	CONN, AMPHENOL, 57-20360	J808	

J805

PIN	DESCRIPTION
A	CHASSIS GRD
B	LOCKOUT INPUT
C	
D	115VAC 60CY
E	115VAC 60CY
F	
G	CIRCUIT GRD

J807

PIN	DESCRIPTION
A	CHASSIS GRD
B	REF LOCKOUT
C	CIRCUIT GRD
D	SYNCHRO DET MON
E	S2E
F	
H	FROM XFMR & FAN
J	S2E
K	
L	FROM FUSE TO PWR S-1
M	S2E
N	CLOCK OUT
P	+24V
R	S2F
S	DATA OUT
T	-24V
U	TO REF & BP LIGHTS
V	REF CARRIER OUT
W	-24V PHASE LIGHT
X	INPUT

P808

PIN	DESCRIPTION
1	A
2	A1 (DATA)
3	A2, A3, A4
4	B
5	B1, B4
6	B2, B3
7	B2, B3
8	C
9	C1, C4
10	C2
11	C3
12	S3D
13	S3D2
14	S3D1
15	S4E
16	S4E
17	S4E
18	S4E
19	INTEGRATOR
20	GRD
21	+ SET METER-DATA
22	- SET METER-DATA
23	+ ØERROR METER-DATA
24	- ØERROR METER-DATA
25	+ SET METER-REF
26	- SET METER-REF
27	+ ØERROR METER-REF
28	- ØERROR METER-REF
29	55A FROM LOOP FILTER
30	55A, FROM Ø COMP
31	55B METER CAP
32	55B, FROM METER BD
33	54A FROM LOOP FILTER
34	54A, FROM Ø COMP
35	54B METER CAP
36	54B, FROM METER BD

CODE SELECTOR
LMS SWITCH
DATA INVERT SWITCH
DATA SET/OPERATE
REF SET/OPERATE

J801, J802, J803, J804

PIN	DESCRIPTION
CENTER	SIGNAL
SHIELD	GROUND

NOTES:
1) THE GPD-6 FITS INTO A STANDARD RETMA 19" RACK.
2) # = SHIELDED CABLE.
3) #J807 CONSISTS OF THE FOLLOWING: RG-24/U IS USED FOR #24 W.E.G. QTY IS RCD X60-1, RMD-26-1, YOC-074 AND B-0551 ARE ASSEMBLED AND USED FOR RG-196/U CABLE QTY. AS REQ'D EACH

REF	DESCRIPTION	QTY

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

	GPD-6
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON
XXX .010
XX .020
FRACTIONS 1/32
ANGLES 1°
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS 81401B CLASS 1
BREAK ALL CORNERS AND EDGES
REMOVE BURRS .015 MAX
MATERIAL
FINISH

CONTRACT NO
DRAWN R T 11/22/66
CHECKED 11/1/67
DESIGNER 11/1/67
PROJECT ENG. 11/1/67
APPROVED R T 11/2/67
APPROVED
APPROVED

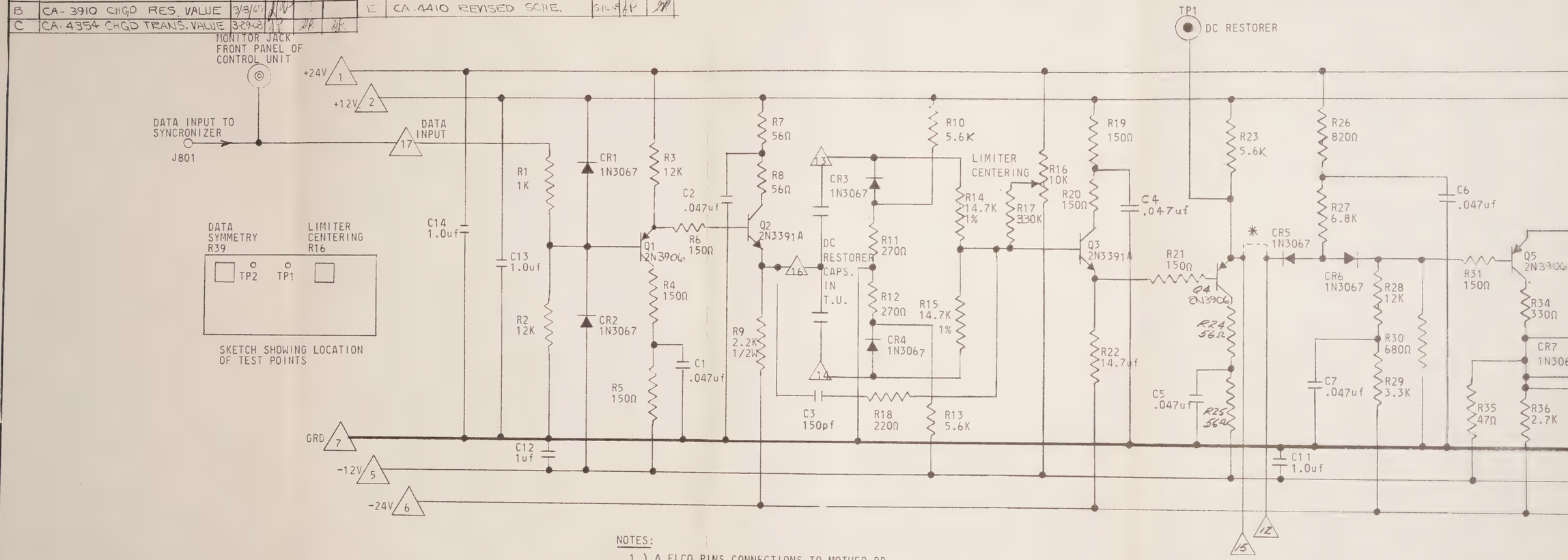
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN

OUTLINE DWG GPD-6

SIZE	CODE IDENT	DO-015272-.D
D	08539	

SCALE
SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-3910 CHGD RES. VALUE	3/8/67			
C	CA-4354 CHGD TRANS. VALUE	3/29/68			
D	CA-4413 CHGD R45 VALUE	4/19/68			
E	CA-4410 REVISED SCHE.	5/6/68			



NOTES:

1.) Δ ELCO PINS CONNECTIONS TO MOTHER BD.

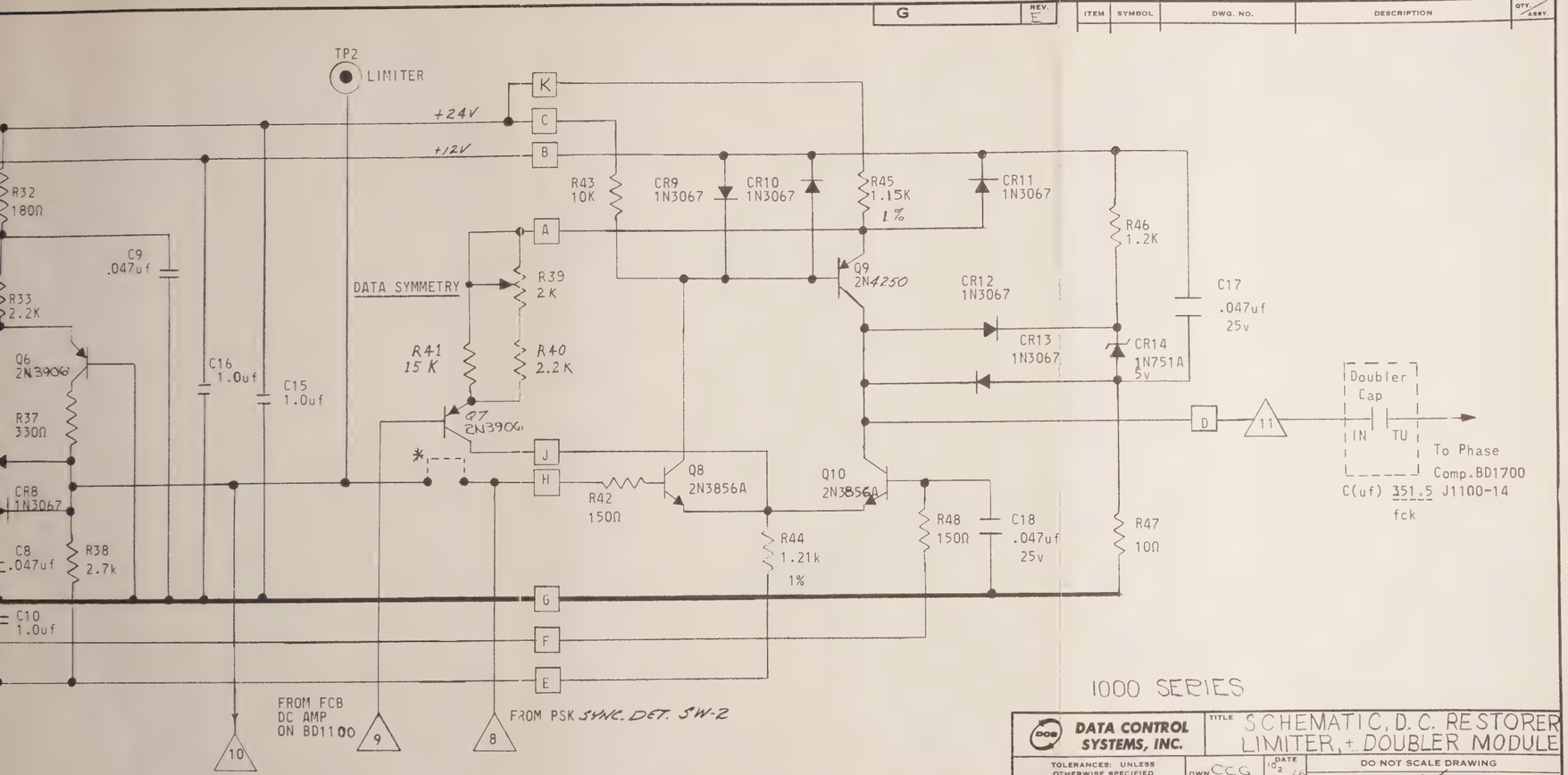
2.) REF. ASSY TA-015166

3.) REF. BLOCK DIAGRAM DB-015327

4.) RESISTORS AB,CB,1/4W,10% UNLESS OTHERWISE NOTED..

5.) P/N-15166-1 DESIGNATES THE USE OF THESE TWO JUMPERS P/N-15166-1 IS TO BE USED IN THE GPS-586 ONLY. P/N-15166-2 DESIGNATES THE OMISSION OF THESE TWO JUMPERS AND IS USED IN THE GPD-6 ONLY.

REF.	DESCRIPTION	QTY



1000 SERIES

G	E	ITEM	SYMBOL	DWG. NO.	DESCRIPTION

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, D.C. RESTORER LIMITER, + DOUBLER MODULE

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED

		DATE
DWN. CCG		10/2/66
CHKD.		4/26/67
ENG.		6/13/67
APP.		6/21/67
SCALE		

DO NOT SCALE DRAWING
MAT'L
FINISH

GW-015532 REV. E

SHEET

GPD-6 FIRST PRODUCT | NEXT ASSEMBLY | REF QTY. ASSY.

REV	DESCRIPTION	DATE	DWN	CHK.	APP.
B	CA-4003 CHG TRANS TYPE	9/6/68	[illegible]	[illegible]	MR
C	CA-4263 CHG. R1138 FROM 3.3 TO 332	2/6/69	[illegible]	MR	MR
D	CA-4442 ADDED C *, R1170, C.2.	2/26/69	BR	MR	MR

TW-015284 REV C

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY ASSY.

NOTES:
1. ○ TERMINALS ON VCO DC AMP BD 1100
2. ○ TERMINALS ON PHASE COMPARATOR BD 1700
3. REF ASSY GA-015154
4. BLOCK DIAGRAM DB-015327
5. △ ELCO CONNECTION TO MOTHER BD
6. * Q1105 TO USE 2N3638 ONLY, NO SECOND CHOICE.

PHASE ERROR METER

FROM PHASE COMP BD-1700

OPERATE / SET

MODE SWITCH ON CONTROL UNIT

LOOP FILTER IN T.U.

TO PHASE COMP BD-1700

FCB

J1100-8

J1100-1 +24V
J1100-2 +12V
J1100-3 +8V
J1100-11
J1100-13
J1100-7 GRD
J1100-4 -8V
J1100-5 -12V
J1100-6 -24V

C1124 1.0μf
C1123 1.0μf
C1122 1.0μf
C1121 1.0μf
C1120 1.0μf
C1119 1.0μf

R1148 20K PHASE COMP. ZERO
R1149 1K
R1145 1K
R1143 390K
R1140 100K
R1147 220Ω
R1142 220Ω
R1141 47K
R1139 10K FCB ZERO AMP
R1138 3.3K
R1137 220Ω
R1136 10K
R1134 3.3K
R1135 2.2K ½W
R1133 3.16K
R1132 2.87K
R1130 150Ω
R1131 10K
R1150 10K
R1196 220K

C1111 2Mmf NOM
C1112 1000μμf
C1110 .047μf
C1108 68 μμf
C1109 .047μf

Q1111 2N3391A
Q1110 2N3391A
Q1109 2N4250
Q1108 2N3393A
Q1107 2N2218 OR TN52

CR1113 IN3067
CR1112 IN3067
CR1111 IN3067
CR1110 2N3640
CR1109 IN3067

TP1101 FCB

TO INTEG. & DOUBLER FCB J1100-10

C1106 .47μf

R1129 10Ω

R1102 1.05K ½W
R1106 330Ω
R1105 500Ω VCO FREQ RANGE
R1107 4.7Ω
R1103 1.47K
R1101 4.7K
R1109 470Ω

Q1101 2N3638

C1101 470μμf
R1109 1.2K
Q1104 2N3391A
R1110 316Ω
CR1103 IN3067
C1102 .047μf
R1111 5.6K
R1112 316Ω
R1113 100Ω
R1114 12K

J1100-9 -12V -24V FREQ ADJ IN T.U.

J1100-17 J1100-14 VCO TIMING CAP IN T.U.
R1119 732Ω
R1121 150Ω

VCO SYM R1115 10K

R1116 1.97K
R1117 226.1Ω
R1118 226.1Ω
CR1101 IN2941A
CR1102 IN2941A

R1102 2N4250
Q1103 2N4250

R1108 56Ω

R1123 100Ω
R1122 1K
C1105 .047μf
R1124 1.0K
R1125 1.0K
R1126 220Ω
C1109 68μμf
CR1105 IN3600
CR1106 IN3600
CR1107 IN751A
CR1108 IN751A
Q1106 2N3638

R1120 1.33K
R1127 150Ω
R1128 68Ω
C1103 .047 MF
Q1105 2N3638 *

TO VCO QUAD CIRCUIT BD-1700 (1 - 6)
TO METER AMP BD-1700 (2 - 9)
TO VCO DRIVERS J1100-15 BD-1200

+24V +12V +8V -8V -12V -24V

TERMINAL BOARD
R1113 R1105 R1149 R1139 TP1101
0 1 0 2 0 3

SKETCH SHOWING LOCATION & IDENTIFICATION OF TERMINALS & TEST POINTS.

REF	DESCRIPTION	QTY

GPD-6 FIRST PRODUCT

NEXT ASSEMBLY

REF QTY

1100 SERIES

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, VCO, DC AMP

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC ± 1/64 ANG ± 0°30'
FLATNESS WITHIN ~ IN.
FRACTIONAL HOLES -0 + 1/64
NOTE BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT ~

DO NOT SCALE DRAWING

		DATE
DWN	C C G	10-7-66
CHKD	[illegible]	4-3-67
ENG	[illegible]	6-14-67
APP	[illegible]	6-16-67

MAT'L

FINISH

SCALE

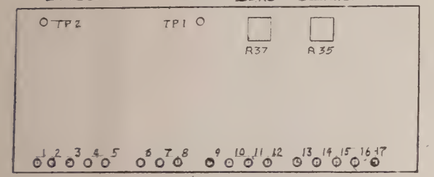
TW-015284 REV C

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-3982 ADD NOTE #1	11/1/67			
C	CA-4413 CHG'D COMP. SERIES	4-9-68			

8)-1 INDICATES GPS-5&6
" " " GPD-6

ø METER VCO QUAD. SYMMETRY

DOUBLER PCB ZERO



SKETCH SHOWING LOCATION & IDENTIFICATION OF TERMINALS & TEST POINTS.

NOTES
* 1)-1 DESIGNATES THE USE OF CR-9 & CR10.
2)-2 " " OMISSION OF CR9 & THE REPLACEMENT OF CR10 WITH #22 BUSS JUMP.

2.△ ELCO PIN CONN ON VCO BD1100 TO MOTHER BD
3.○ TERMINALS ON VCO BD
4. REF. ASSY GA-015155
5. REF. BLOCK DIAGRAM DB-015327
6.○ TERMINAL ON ø COMP BD
7. RESISTORS ARE AB, CB, ¼W, 10% UNLESS OTHERWISE NOTED.

REF.	DESCRIPTION	QTY.

TW-015280

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY. ASSY.

1700 SERIES

DATA CONTROL SYSTEMS, INC.

TITLE SCHEMATIC, PHASE COMPARATOR

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG ± 0°30'
FLATNESS WITHIN ~/IN.
FRACTIONAL HOLES Ø .0 + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT

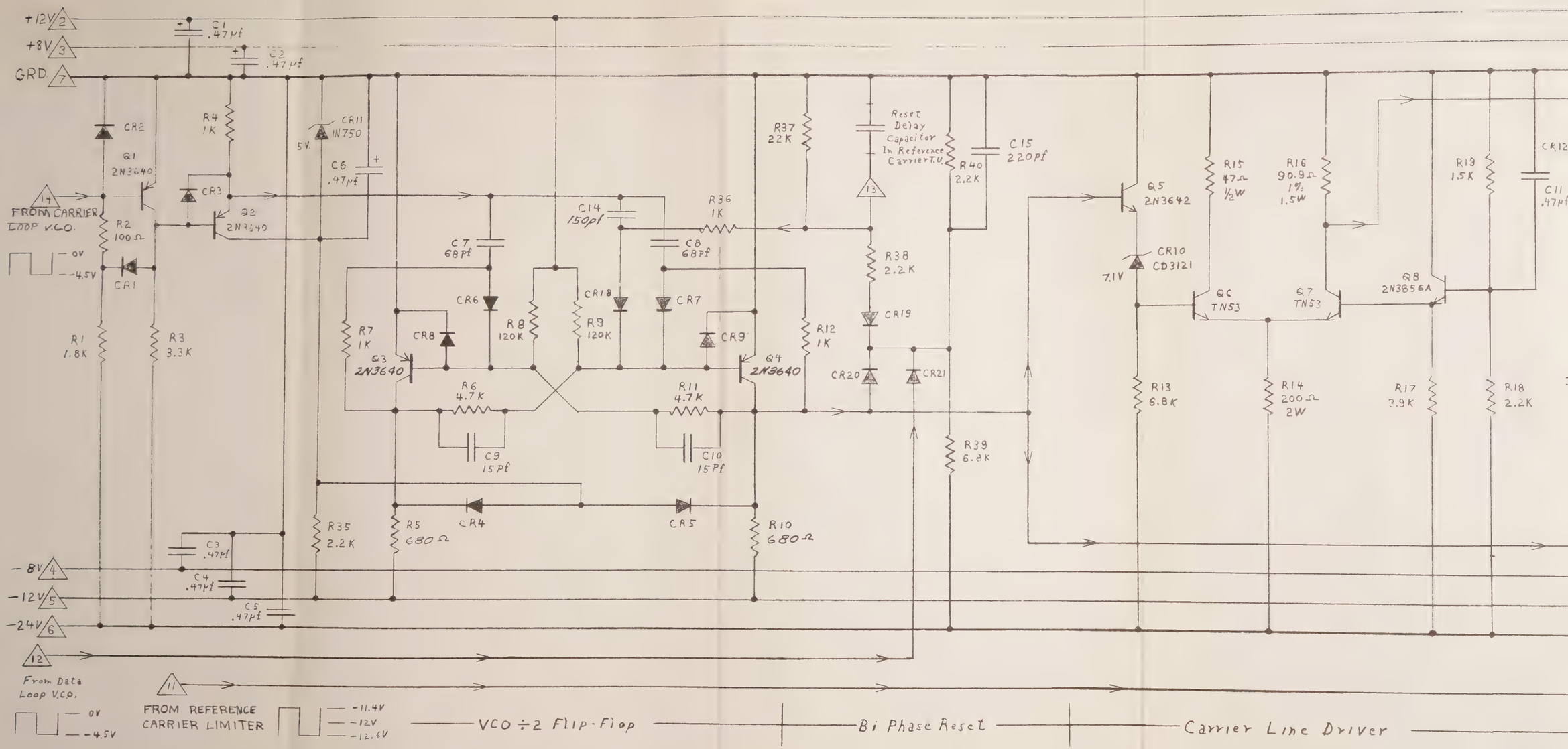
DO NOT SCALE DRAWING

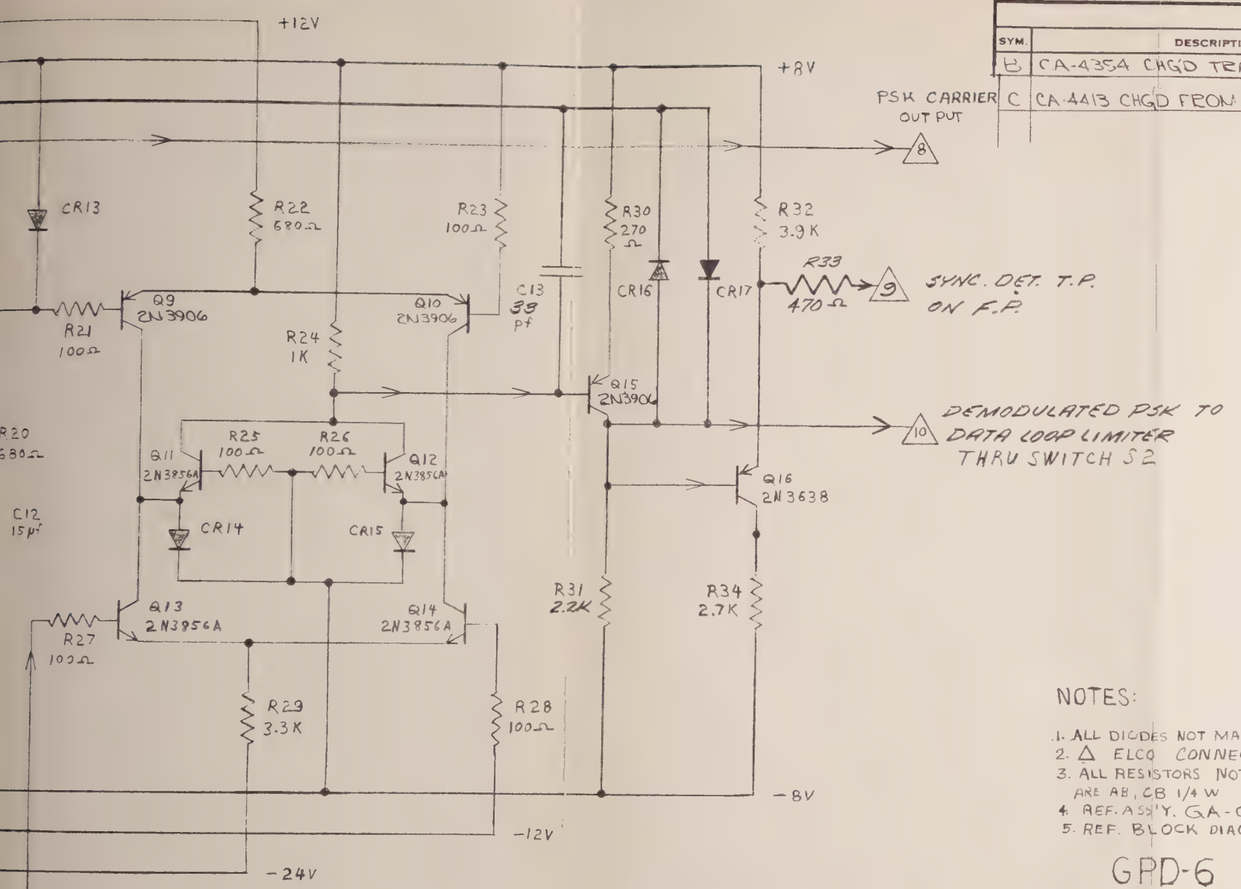
		DATE
DWN.	C.C.G	10-20-67
CHK'D		4/9/67
ENG.		10/17/67
APP.		9/9/67
SCALE		

MAT'L
FINISH

TW-015280 REV. C

GPS-5&6			
GPD-6			
FIRST PRODUCT	NEXT ASSEMBLY	QTY	


+12V 2
+8V 3
GRD 7
C1 .47μf
C2 .47μf
CR2
R4 1K
CR11 IN750 5V.
C6 .47μf
Q1 2N3640
CR3
Q2 2N3640
14 FROM CARRIER LOOP V.C.O.
R2 100Ω
0V
-4.5V
CR1
R1 1.8K
R3 3.3K
C14 150pf
R36 1K
C7 68pf
C8 68pf
CR6
CR18
CR7
R7 1K
CR8
R8 120K
R9 120K
CR9
R12 1K
Q3 2N3640
Q4 2N3640
R6 4.7K
R11 4.7K
C9 15pf
C10 15pf
CR4
CR5
R35 2.2K
R5 680Ω
R10 680Ω
C3 .47μf
C4 .47μf
C5 .47μf
-8V 4
-12V 5
-24V 6
12
From Data Loop V.C.O.
0V
-4.5V
11
FROM REFERENCE CARRIER LIMITER
-11.4V
-12V
-12.6V
R37 22K
Reset Delay Capacitor In Reference Carrier T.U.
13
R40 2.2K
C15 220pf
R38 2.2K
CR19
CR20
CR21
R39 6.8K
Q5 2N3642
CR10 CD3121 7.1V
Q6 TN53
Q7 TN53
Q8 2N3856A
R15 47Ω 1/2W
R16 90.9Ω 1% 1.5W
R13 6.8K
R14 200Ω 2W
R17 3.9K
R13 1.5K
R18 2.2K
CR12
C11 .47μf
VCO ÷2 Flip-Flop
Bi Phase Reset
Carrier Line Driver



Synchronous Detector

REVISIONS					
SYM.	DESCRIPTION	DATE	BY	CHK'D	APP'D
B	CA-4354 CHG'D TRANS TYPES & VALUE	3-29-68			
C	CA-4413 CHG'D FROM 1700'S TO 1800'S	4-19-68			

NOTES:

1. ALL DIODES NOT MARKED ARE IN3067'S
2. △ ELCO CONNECTION
3. ALL RESISTORS NOT OTHERWISE MARKED ARE AB, CB 1/4 W
4. REF. ASS'Y. GA-015151
5. REF. BLOCK DIAGRAM DB-015327

GPD-6 1800 SERIES

DATA CONTROL SYSTEMS, INC.

TITLE SCHEMATIC, SYNCHRONOUS DETECTOR AND PSK CARRIER LINE DRIVER

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015"

		DATE
DWN.	CCG	11/13/66
CHK'D		6/13/67
PROJ. ENG.		6/13/67
CH. ENG.		6/14/67
SCALE		

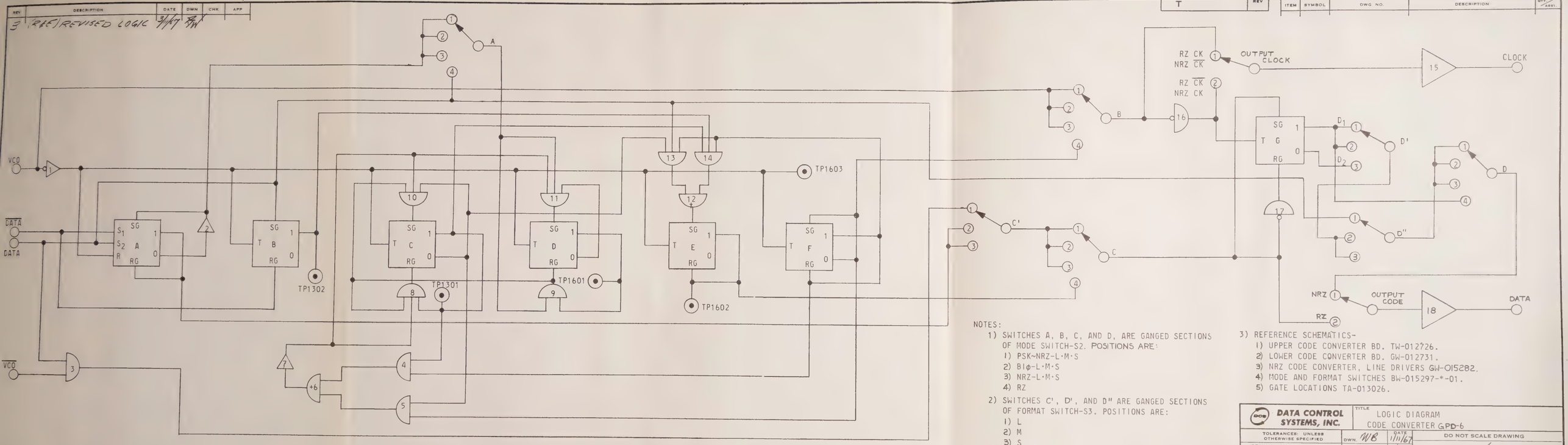
DO NOT SCALE DRAWING
MAT'L
FINISH

RW-015283 C

REV	DESCRIPTION	DATE	DWN	CHK	APP
3	(R&E) REVISED LOGIC	3/1/67	BK		

REV
T

ITEM	SYMBOL	DWG NO.	DESCRIPTION	QTY ASSY.



NOTES:

1) SWITCHES A, B, C, AND D, ARE GANGED SECTIONS OF MODE SWITCH-S2. POSITIONS ARE:
   1) PSK-NRZ-L·M·S
   2) BIφ-L·M·S
   3) NRZ-L·M·S
   4) RZ
2) SWITCHES C', D', AND D" ARE GANGED SECTIONS OF FORMAT SWITCH-S3. POSITIONS ARE:
   1) L
   2) M
   3) S
3) REFERENCE SCHEMATICS-
   1) UPPER CODE CONVERTER BD. TW-012726.
   2) LOWER CODE CONVERTER BD. GW-012731.
   3) NRZ CODE CONVERTER, LINE DRIVERS GW-015282.
   4) MODE AND FORMAT SWITCHES BW-015297-*-01.
   5) GATE LOCATIONS TA-013026.

DESCRIPTION	QTY

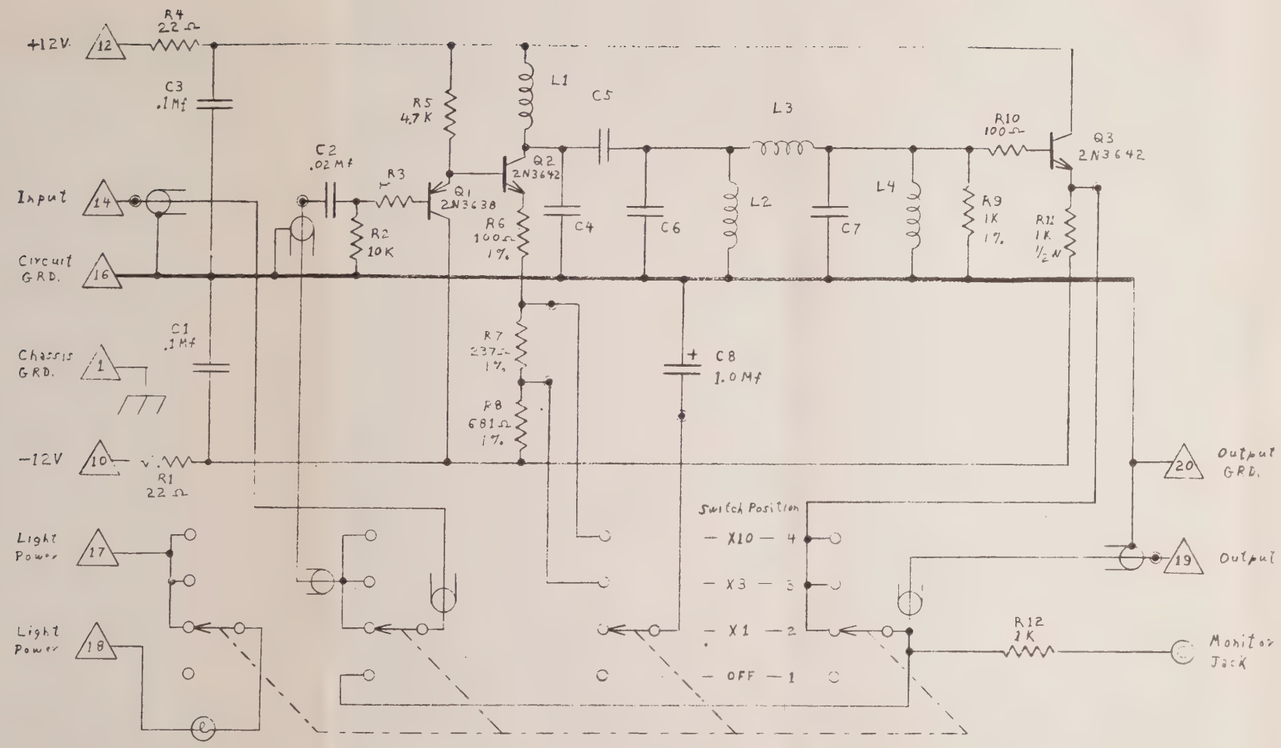
FIRST PRODUCT	NEXT ASSEMBLY	QTY. ASSY.

DATA CONTROL SYSTEMS, INC.

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES .0 + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

TITLE: LOGIC DIAGRAM
CODE CONVERTER GPD-6

DWN. WB	DATE 1/11/67	DO NOT SCALE DRAWING
CHK'D		MAT'L ~
ENG.		FINISH ~
APP. RT	1/12/67	
SCALE ~		TY-015731 REV. B
		SHEET

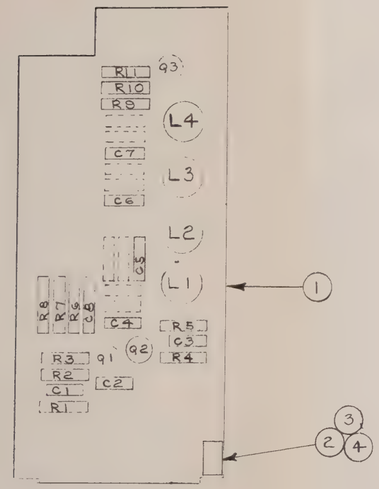


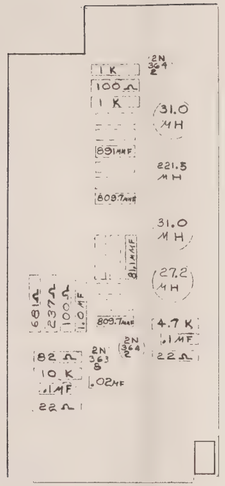
NOTES:

1) UNMARKED COMP ARE FREQ SENS. SEE BOARD ASSY TA-016003

2) 1% RES. ARE ELECTRA, MFSC-D, ¼W ALL OTHERS ARE AB, CB, ¼W, 10% UNLESS OTHERWISE MARKED.

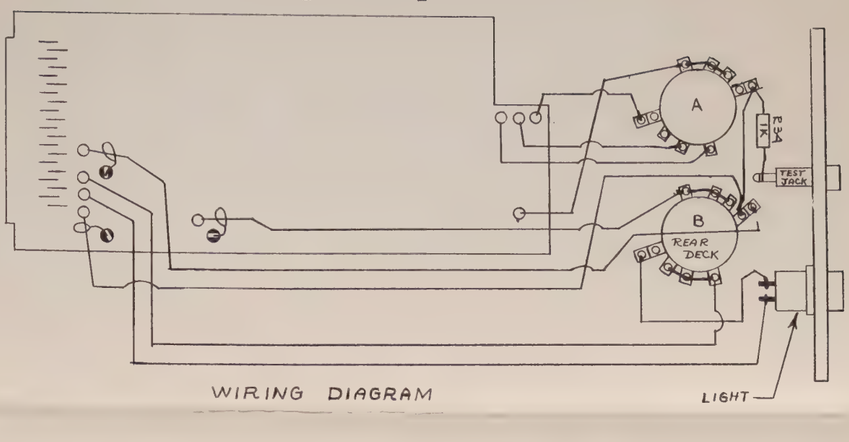
DATA CONTROL SYSTEMS, INC.	SCHEMATIC GPD-6/EP	
	TA-016005	REV A





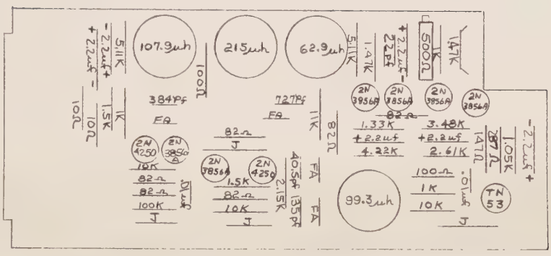
	R1		RES. A.B.C.B. 1/4 W 10% 22Ω	1
	R2		10K	1
	R3		82Ω	1
	R4		22Ω	1
	R5		4.7K	1
	R6		ELECTRA MF5C-D 1/4W, 1% 100Ω	1
	R7		237Ω	1
	R8		681Ω	1
	R9		A.B.C.B. 1/4W. 10% 1K	1
	R10		100Ω	1
	R11		1K	1
	C1		CAP. RMC DISCAP +80 -20 % 100V .1MF	1
	C2		.02MF	1
	C3		.1MF	1
	C4		DURMICA, DM15, 300V 1% 850pf	1
	C5		85.6pf	1
	C6		850pf	1
	C7		100V 1% 936pf	1
	C8		SPRAGUE, 150D, 20V, 20% 1.0 MF	1
	Q1		TRANS. 2N 363A	
	Q2		2N 3642	
	Q3		2N 3642	
	L1	BA-018002	INDUCTOR 27.2 uh	1
	L2	BA-018002	INDUCTOR 31.0 uh	1
	L3	BA-018002	INDUCTOR 221.5 uh	1
	L4	BA-018002	INDUCTOR 31.0 uh	1
1		CF-016002	BOARD FAB	1
2		BD-011021	BLOCK GUIDE	1
3			SCREW #2-56-2A x 3/16 PHMS SCP	2
4		BD-013635	PLATE, WASHER	1
ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY REQ'D

GPD-6/BP
1.024 MHz ± 260 KHz

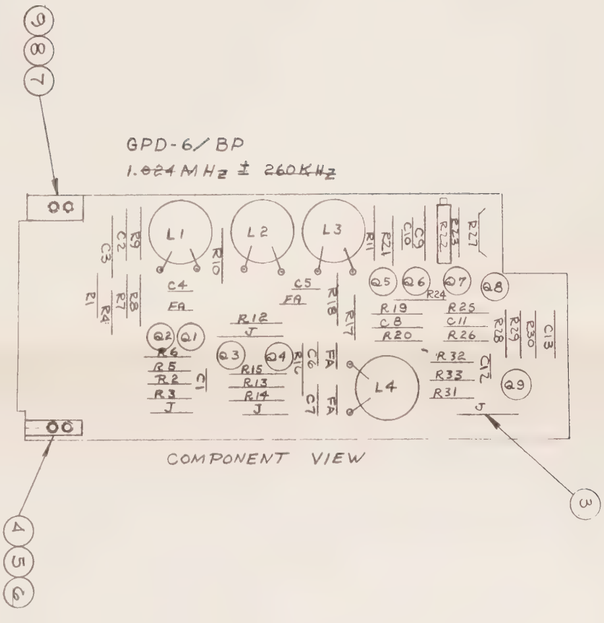


WIRING DIAGRAM

GPD-6/BP
1.024 MHz ± 260 KHz



COMPONENT VIEW



COMPONENT VIEW

ITEM	SYMBOL	PART NO.
1		
2		
3		
4	Q9	BD-011021
5	Q8	BD-013635
6	Q7	AS-826028-*
7	Q6	BD-008927
8	Q5	BD-009837
9	Q4	AS-826028-*
	Q3	
	Q2	
	Q1	
	L4	BA-017611
	L3	BA-017611
	L2	BA-017611
	L1	BA-017611
	C13	
	C12	
	C11	
	C10	
	C9	
	C8	
	C7	
	C6	
	C5	
	C4	
	C3	
	C2	
	C1	
	R34	

			RES. AB,CB, 1/4W, 10%,	1K
			CAP RMC DISCAP ±80-20 TA, 100V .01uf	
			SPRAGUE, 150-D, ±20%, 20V, 2.2uf	
			SPRAGUE, 150-D ±20%, 20V, 2.2uf	
			DURMICA, DM-10, 100V, 1% 389pf	
			DURMICA, DM-15, 100V, 1% 727pf	
			DURMICA, DM-10, 100V, 1% 40.5pf	
			DURMICA, DM-10, 100V, 1% 135pf	
			SPRAGUE, 150-D ±20% 20V 2.2uf	
			SPRAGUE, 150-D ±20% 20V, 2.2uf	
			DURMICA, DM-10, 100V, 22pf	
			SPRAGUE, 150-D ±20%, 20V, 2.2uf	
			RMC DISCAP ±80-20 TA, 100V .01 uf	
			SPRAGUE, 150-D ±20% 20V 2.2uf	
			INDUCTORS,	107.9uh
				215 uh
				62.9uh
				99.3uh
			TRANS. GE	2N3856A
			FAIRCHILD	2N4250
			GE	2N3856A
			FAIRCHILD	2N4250
			GE	2N3856A
				2N3856A
				2N3856A
				2N3856A
			SPRAGUE	TN53
			BLOCK GUIDE	
			PLATE WASHER	
			SCREW #2-56	
			BLOCK, GUIDE	
			PLATE WASHER	
			SCREW #4-40, PHMS	

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY. REQ'D
1		GW-017475	SCHEMATIC	REF
2		CF-017474	BD. FAB,	REF
3	J		JUMPERS, BUSS #22 AWG, / TEFLON SLEEVING	A/R
	R1		RES., AB, CB, 1/4W, 10% 10Ω	1
	R2		82Ω	1
	R3		100K	1
	R4		10Ω	1
	R5		82Ω	1
	R6		10K	1
	R7		1.5K	1
	R8		ELECTRA, MF5C-D, 1% 1K	1
	R9		5.11K	1
	R10		100Ω	1
	R11		5.11K	1
	R12		AB, CB, 1/4W, 10% 82Ω	1
	R13		82Ω	1
	R14		10K	1
	R15		1.5K	1
	R16		ELECTRA, MF5C-D, 1%, 2.15K	1
	R17		AB, CB, 1/4W, 10% 82Ω	1
	R18		ELECTRA, MF5C-D, 1%, 11K	1
	R19		ELECTRA, MF5C-D, 1%, 1.33K	1
	R20		ELECTRA, MF5C-D, 1%, 4.32K	1
	R21		ELECTRA, MF5C-D, 1%, 1.47K	1
	R22		POT, BOURNS 3007P-1-501, 500Ω	1
	R23		ELECTRA, MF5C-D, 1%, 1K	1
	R24		AB, CB, 1/4W, 10% 82Ω	1
	R25		ELECTRA, MF5C-D 1% 3.48K	1
	R26		2.61K	1
	R27		1.47K	1
	R28		147Ω	1
	R29		287Ω	1
	R30		1.05K	1
	R31		10K	1
	R32		AB, CB, 1/4W, 10% 100Ω	1
	R33		AB, CB, 1/4W, 10% 1K	1

NOTES:
1) * = LATEST REVISION
2) ** = SCREW LENGTHS TO BE DETERMINED IN ACCORDANCE WITH DCS WORKMANSHIP MANUAL #AS-832011.

DATA CONTROL SYSTEMS, INC.

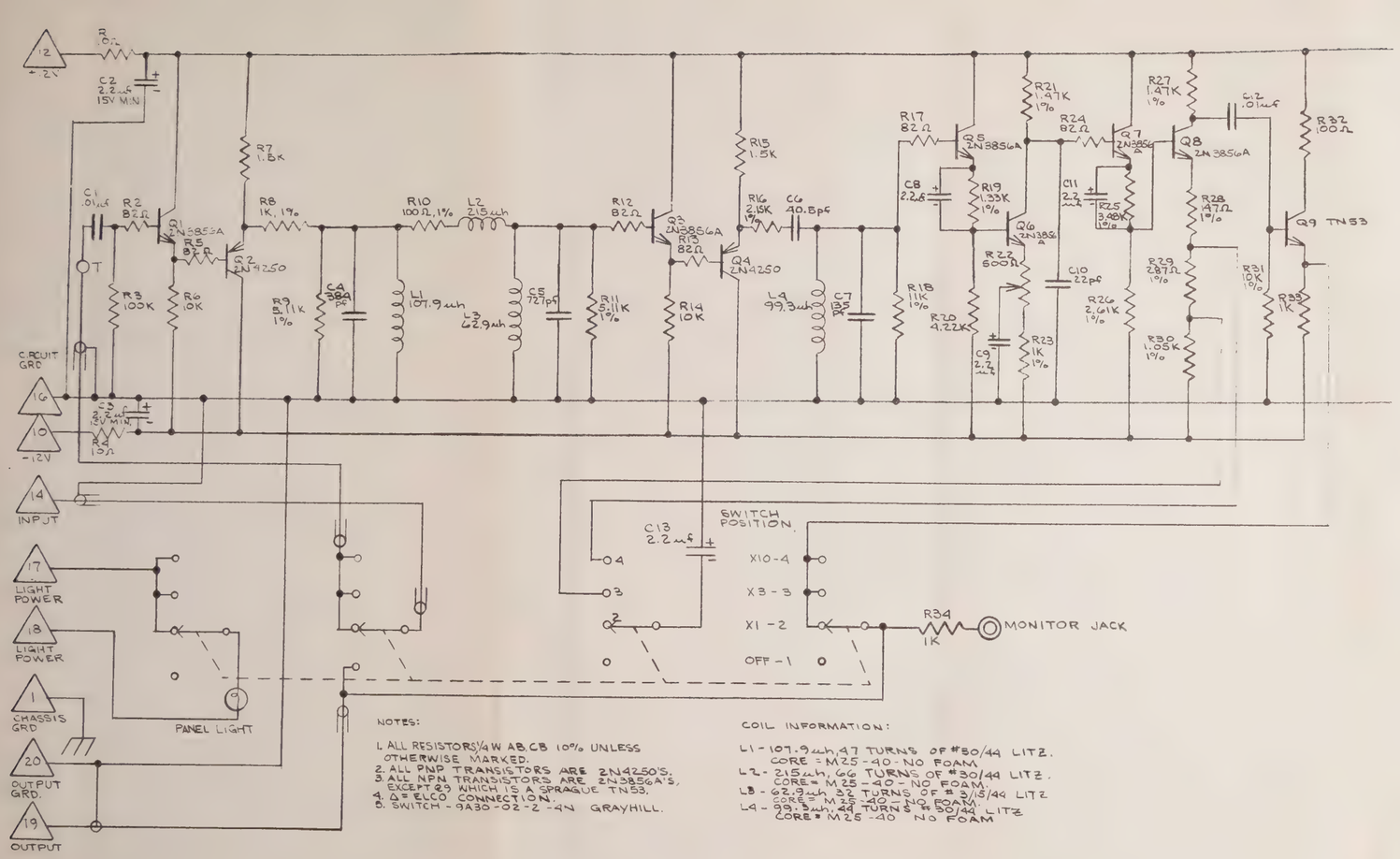
TITLE: BD. ASS'Y, BANDPASS FILTER 1.024MHz ± 260KHz - GPD-6/BP

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015"

DWN. J.E. HOLZE 2/8/68
CHKD. 2/28/68
PROJ. ENG. 2/28/68
CH. ENG. RT 2/68
SCALE

DO NOT SCALE DRAWING
MAT'L
FINISH

RA-017476 REV. A



NOTES:

1. ALL RESISTORS 1/4W AB.CB 10% UNLESS OTHERWISE MARKED.
2. ALL PNP TRANSISTORS ARE 2N4250'S.
3. ALL NPN TRANSISTORS ARE 2N3856A'S, EXCEPT Q9 WHICH IS A SPRAGUE TN53.
4. Δ = ELCO CONNECTION.
5. SWITCH - 9A30-02-2-4N GRAYHILL.

COIL INFORMATION:

L1 - 107.9uh, 97 TURNS OF #30/44 LITZ. CORE = M25-40-NO FOAM
L2 - 215uh, 66 TURNS OF #30/44 LITZ. CORE = M25-40-NO FOAM
L3 - 62.9uh 32 TURNS OF # 5/15/44 LITZ CORE = M25-40-NO FOAM.
L4 - 99.3uh, 44 TURNS # 30/44 LITZ CORE = M25-40 NO FOAM

REVISIONS

SYM.	DESCRIPTION	DATE	BY	CHK'D	APP'D

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, BANDPASS FILTER 1.024MHz ± 26CKHz

TOLERANCES: UNLESS OTHERWISE SPECIFIED			
DECIMAL - 3 PLACE ± .005	DWN	[illegible]	2-28-68
DECIMAL - 2 PLACE ± .010	CHK'D.	[illegible]	2/28/68
FRAC. ± 1/64 ANG. ± 0°30'	PROJ.	[illegible]	4-24-68
FLATNESS WITHIN /IN.	ENG.	[illegible]	4-24-68
FRACTIONAL HOLES -0, + 1/64	CH. ENG.	RT	2/68
NOTE: BREAK ALL SHARP			

DO NOT SCALE DRAWING

MAT'L

FINISH

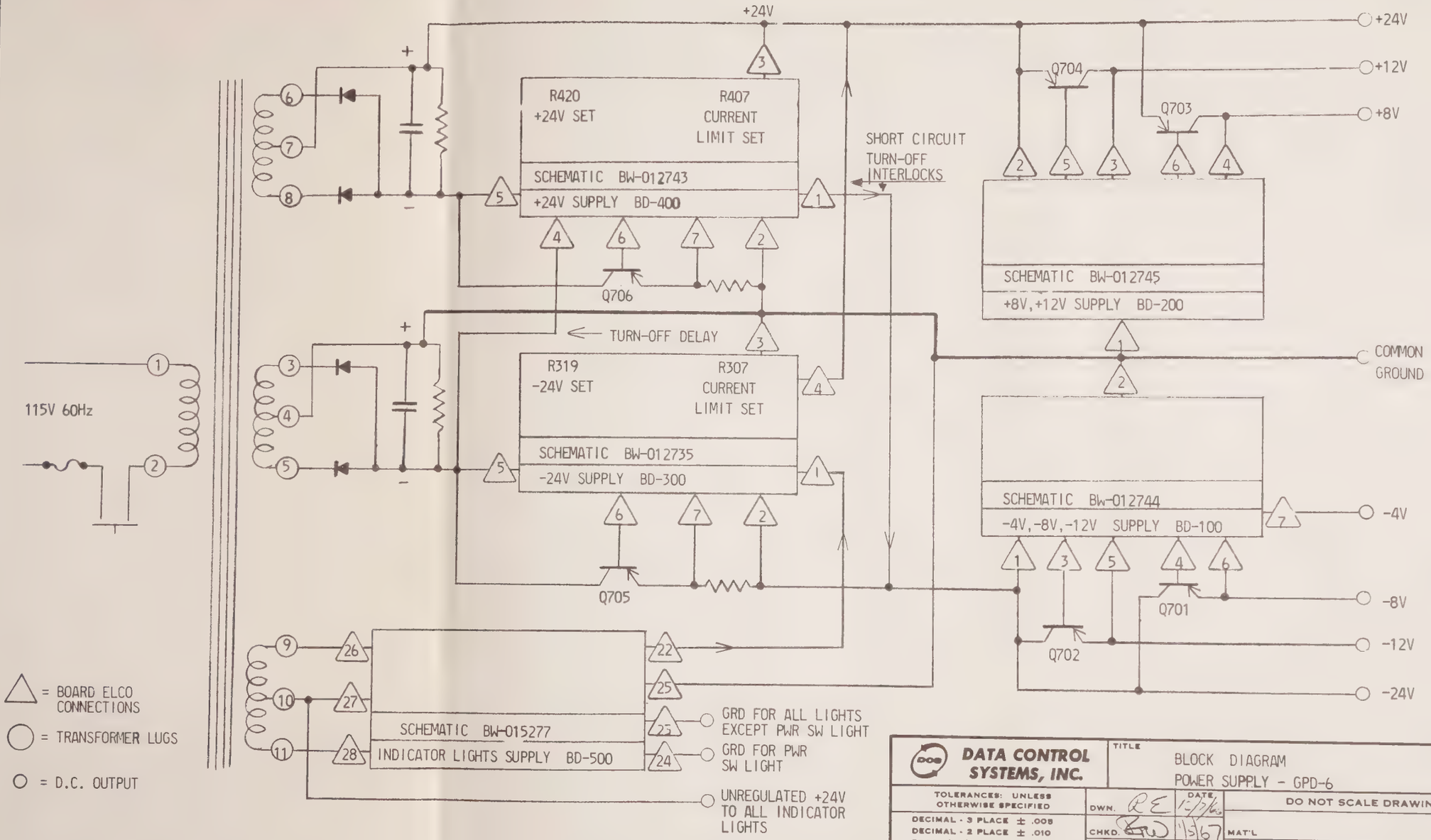
GPD-Co/BP

GW-01745

REV. A

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B					

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY./ASSY



REF.	DESCRIPTION	QTY

GPD-6	———	———
PRODUCT	NEXT ASSEMBLY	QTY./ASSY.

DATA CONTROL SYSTEMS, INC.

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015" SURFACE ROUGHNESS NOT TO EXCEED ✓

		DATE
DWN.	RE	12/26/66
CHKD.	RW	1/5/67
ENG.	[illegible]	1/4/67
APP.	RT	1/12/67
SCALE		

TITLE
BLOCK DIAGRAM
POWER SUPPLY - GPD-6

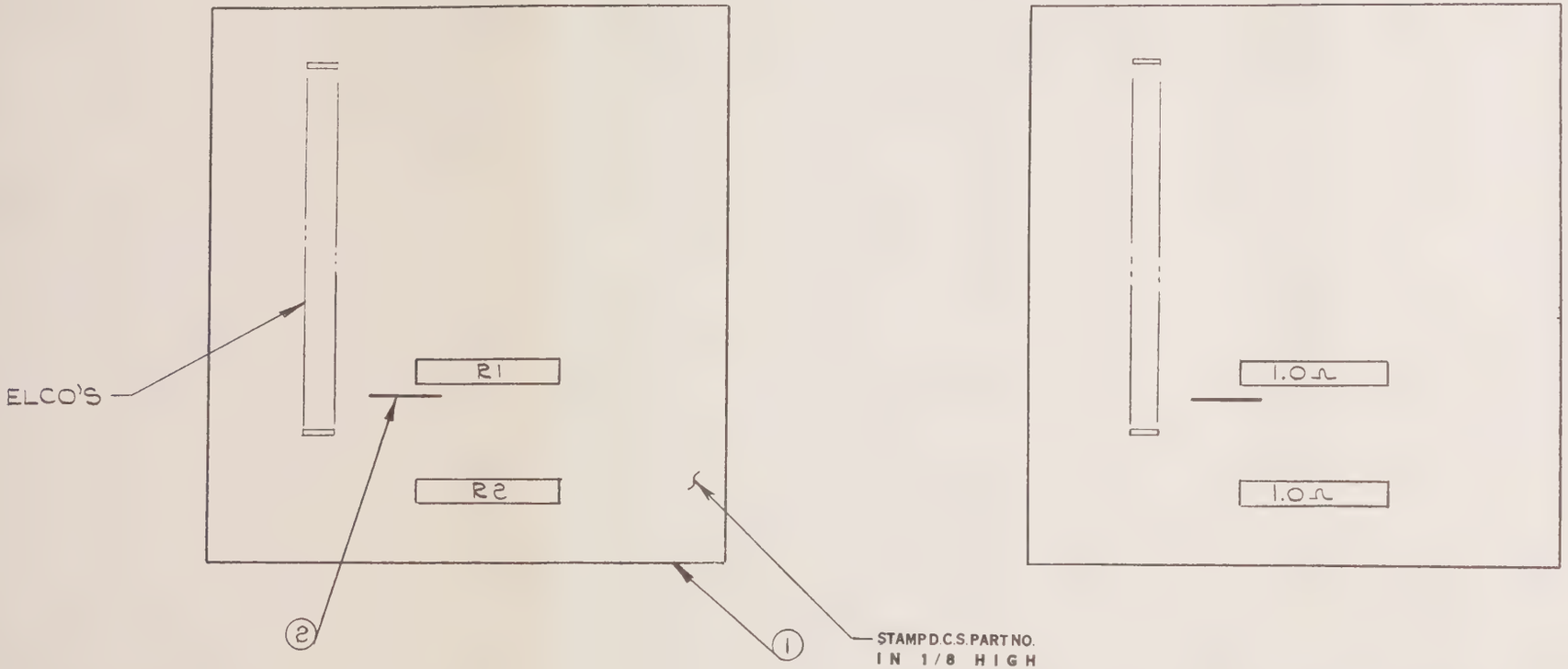
DO NOT SCALE DRAWING
MAT'L
FINISH

B B - 015326 REV. A

SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B					

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY./ASSY.
1		CF-010681	BD FAB, MOTHER PWR. SUPPLY	1
2			JUMPER #22 BUSS	A/R
	R1		RES., MEPCO, 1% P3 1.0Ω	1
	R2		RES., MEPCO, 1% P3 1.0Ω	1



600 SERIES

REF.	DESCRIPTION	QTY

GPD-6 BA-015319

PRODUCT	NEXT ASSEMBLY	QTY./ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE: BD. ASSY, MOTHER POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN — /IN.
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ✓

		DATE
DWN. GB		8/24/66
CHKD. RTW		8/25/66
ENG. H W M		8/25/66
APP. RAe		8/26/66
SCALE —		

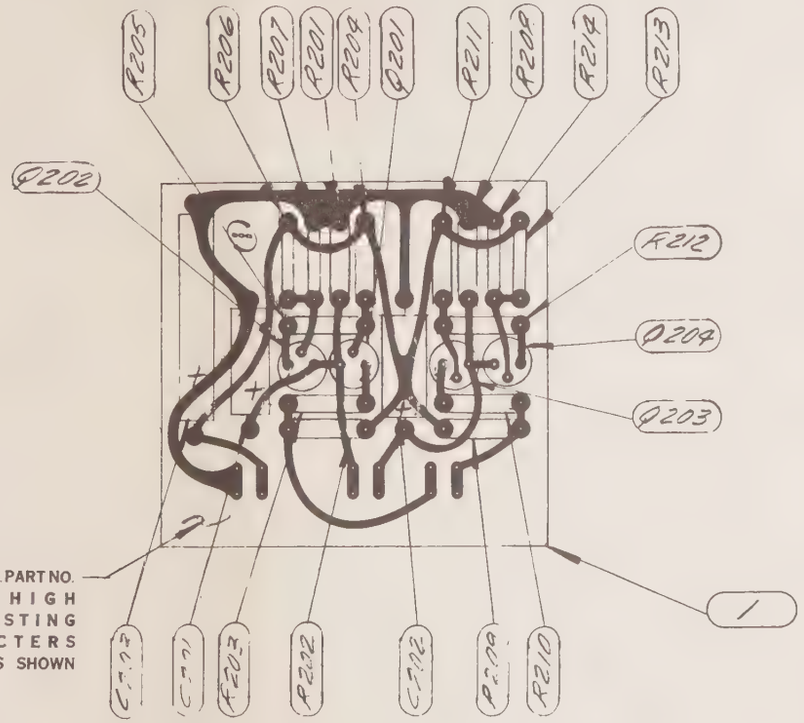
DO NOT SCALE DRAWING
MAT'L
FINISH

BA-015276 REV. A

SHEET

REV	DESCRIPTION	DATE	DWN	CHK	APP
B	SERIES WAS 300 R&E	3/27/64	PJH	RWG	RKT
C	ADDED STAMP P/N NOTE R&E	7/14/64	PJH	WJ	WJ
D	CA-3190-CHG'D. COMPONENTS	3/18/66	P.I.		
E	CA-3929-CHG'D. RES. VALUES	9/19/66	PI		
F	CA-3749 CHG'D COMP. VALUES	5/29/67	JCP		
G	CA-3749-1 CHG Q201 & Q203	1/15/68	JCP	JR	JR
H	CA-4354 CHG'D Q201 & Q203	3 29 68	JP	JR	JR

BA-011460 REV H



ITEM	SYMBOL	DWG NO.	DESCRIPTION	QTY/ASSY
1		BF-010660	BOARD FAB	1
*	R 201		RES. AB, EB, 1/4W, 10%, 4.7K.	1
*	R 202		82Ω	1
*	R 203		120Ω	1
*	R 204		1K	1
*	R 205		1.8K	1
*	R 208		1.8K	1
*	R 209		82Ω	1
*	R 210		150Ω	1
*	R 211		1K	1
*	R 212		2.2K	1
	R 206		RES. T.I, CC1/4, 1/4W, 1% 909Ω	1
	R 207		1.0K	1
	R 213		909Ω	1
	R 214		511Ω	1
	Q 201	NO SECOND CHO:	TRANS, MOTOROLA 2N3906	1
	Q 202		TRANS, G.E, 2N3391A	1
	Q 203	NO SECOND CHOICE	TRANS, MOTOROLA, 2N3906	1
	Q 204		TRANS, G.E, 2N3391A	1
	C 201		CAP. SPRAGUE TE1160 15K, 50MF	1
	C 202		CAP. 15K, 50MF	1
	C 203		CAP. SPRAGUE TE1307 50K, 50MF	1

NOTE

1. * PER MS35093

REF	DESCRIPTION	QTY

PRODUCT	NEXT ASSEMBLY	QTY/ASSY
SPS-5	DA-011452	1

DATA CONTROL SYSTEMS, INC.

TITLE: BOARD ASSY - +8V, +12V, POWER SUPPLY

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES .0 + 1/64
NOTE: BREAK ALL SHARP CORNERS .005' - .015'
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN	PJH	9/19/63
CHK	RKT	9/29/63
ENG	GM/WJ	10/14/63
APP.	WJ	10/14/63
SCALE	FULL	

DO NOT SCALE DRAWING
MAT'L
FINISH

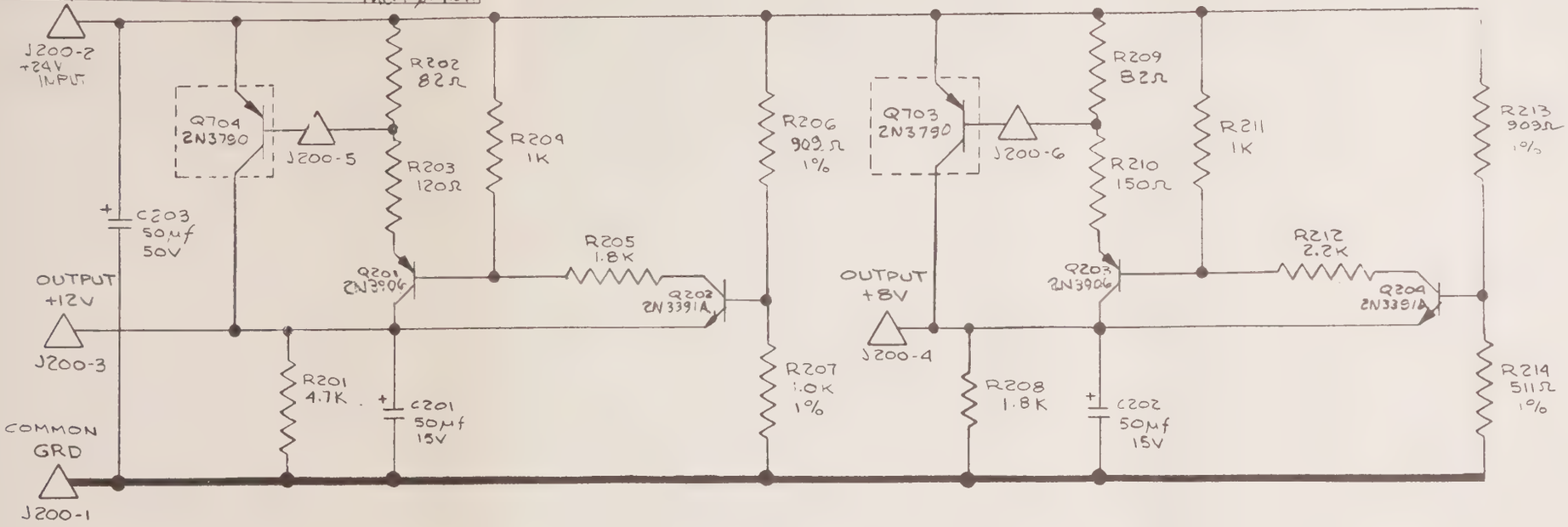
BA-011460 REV H

SHEET

REV.	DATE	DESCRIPTION	BY	CHK'D	APP'D
B	9/23/65	CA-2824- C203 WAS C303	[illegible]	DH	[illegible]
C	3/15/66	CA-3190-CHG'D COMPONENTS	P.I	[illegible]	[illegible]
D	3/1/66	CA-3190-2 CHG'D. Q709, 703 TO 2N3790	P.I	[illegible]	[illegible]
E	3/29/66	CA-3429-CHG'D. RES. VALUES	PI	[illegible]	[illegible]
F	5/23/67	CA-3749 CHG'D COMP. VALUES	[illegible]	[illegible]	[illegible]
G	11/8/68	CA-3749-1 CHG Q201 & Q203	[illegible]	JR	JR
H		CA-435A CHG TRANS TYPE	[illegible]	3/29	JR

BW-012745

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY / ASSY



NOTES:

600

1. △ ELCO PIN CONNECTIONS TO PWR SUP MOTHER BD
2. Q703 & Q704 ARE PART OF ASSY CA-011449
3. REF. ASSY BA-011460
4. REF. BLOCK DIAGRAM DB-013312
5. RESISTORS ARE AB, EB, 1/2W, 10% UNLESS OTHERWISE NOTED.

REF.	DESCRIPTION	QTY

GPS-5	~	~
PRODUCT	NEXT ASSEMBLY	QTY / ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE SCHEMATIC, +8V+12V POWER SUPPLY

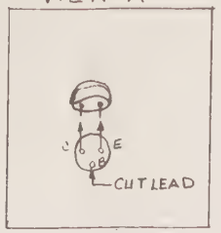
TOLERANCES: UNLESS OTHERWISE SPECIFIED		DATE	DO NOT SCALE DRAWING
DECIMAL - 3 PLACE ± .005	DWN. DH	9/23/64	
DECIMAL - 2 PLACE ± .010	CHKD. [illegible]	1/19/65	MAT'L ~
FRAC. ± 1/64 ANG. ± 0°30'	PROJ. ENG. [illegible]	2/16/66	FINISH ~
FLATNESS WITHIN ~ /IN.	CH. ENG. [illegible]	2/16/66	
FRACTIONAL HOLES -0, + 1/64	SCALE ~		BW-012745 REV. H
NOTE: BREAK ALL SHARP CORNERS .005"-.015"			

REV	DESCRIPTION	DATE	DWN	CHK	APP
C	SERIES WAS 500 CCE	9/24/64	PJH	RWG	RWG
D	R420 WAS 100Ω, Q404 & Q405 WERE 5YL2113 (CCE)	7/14/64	PJH	WJ	WJ
E	CA2621-R402 WAS R403	11/21/64	PJH	RWG	WJ
F	CA-3190- CHG'D. COMPONENTS	3/14/66	P.I.	CD	CD
G	CA-3429 - CHG'D COMA VALUES	9/19/66			
H	CA-3749 CHG'D COMP. VALUES	5/29/67			
J	CA-3913 CHG'D COMP VALUE	9/14/67			
K	CA-3913-1 CHG'D DIODE TYPS	10/27/67			
L	CA-4354 CHG'D TRANS. TYPES & VALUE	3/29/68			

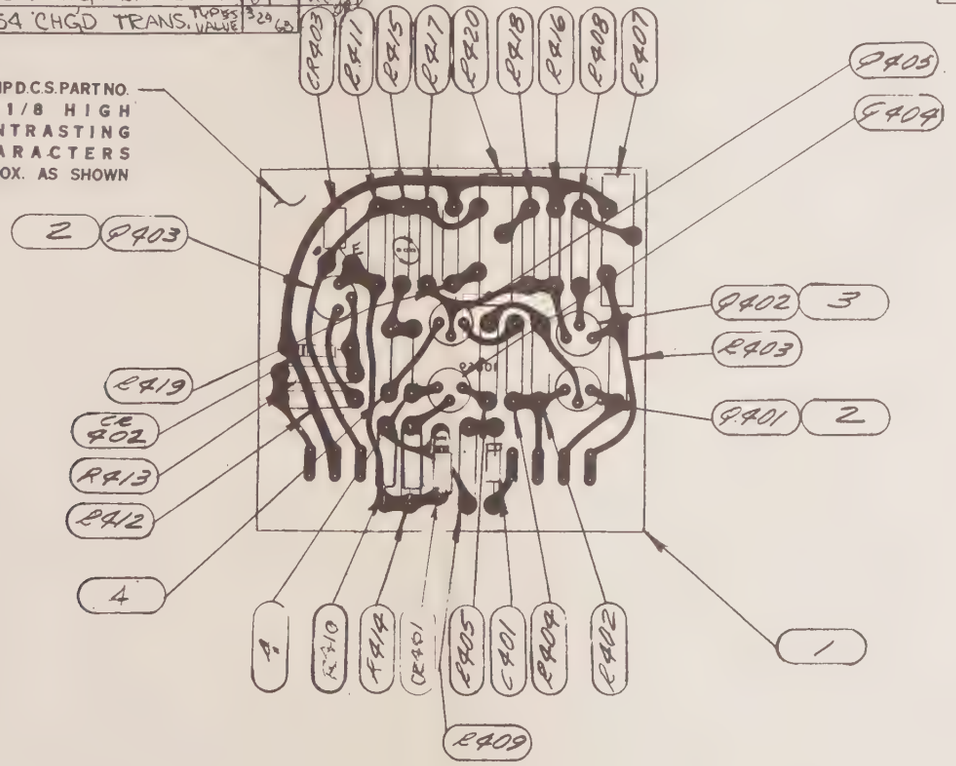
M CA-4340 REVERSE POLARITY OF CR401 — BA-011465 — REV M

NOTE:
1. * PER MS35043

VIEW "A"



STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN



NOTE:
**CR403 TO BE SELECTED AS PER DCS. SPEC. AS-82.1001.

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY
1		BF-010659	BOARD FAB	1
2			PAD MILTON 2055 A10068	2
3			PAD MILTON 2055 A10092	1
*	R402		RES. AB, EB, ½W, 10Ω 1.5K	1
*	R403		100 L.	1
*	R404		2.2K	1
*	R405		2.2K	1
*	R406		220Ω	1
*	R409		5.6K	1
*	R410		39K	1
*	R411		6.8K	1
*	R412		2.2K	1
*	R413		1.2K	1
*	R414		220Ω	1
*	R415		1K	1
*	R419		560Ω	1
	R416		RES. TI, CG ½W, 1%, 1.78K	1
	R417		649Ω	1
	R418		3.16K	1
	R407		TRIMPOT, BOURNS, #3067P-1-501 500Ω	1
	R420		TRIMPOT, BOURNS, #3067P-1-102 1K	1
	C401		CAP, SPRAGUE, 150D, 75V, 20% 0.47 MFD	1
	CR 401		DIODE IN 907	1
	CR 402		DIODE, MOTOROLA, ½M152	1
**	CR 403	SEE VIEW "A"	DIODE, [illegible]	1
	Q401		TRANS, SPRAGUE, TNS3	1
	Q402		TRANS, TI. 2N708 OR G.E. 2N3391A	1
	Q403		TRANS, SPRAGUE, TNS3	1
	Q404	NO SECOND CHOICE	TRANS. [illegible]	1
	Q405		TRANS.	1
4			JUMPER, #22 BUSS WIRE	2

REF.	DESCRIPTION	QTY

PRODUCT	NEXT ASSEMBLY	QTY./ASSY
GPS-5	DA-011452	1

DATA CONTROL SYSTEMS, INC.

TITLE: BD. ASSY, +24V, POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~/IN
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005" - .015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN	PJH	10/15/63
CHKD	WJ	10/15/63
ENG	WJ	10/15/63
APP	WJ	10/15/63
SCALE	FULL	

DO NOT SCALE DRAWING
MAT'L
FINISH

BA-011465 REV M

SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-2824- R402 WAS 1K R CHG'D NOTE 14	3/17/65			
C	CA-3190-CHG'D COMPONENTS	3/18/66	P.I.		
D	CA-3190-2 CHG'D, Q706 TO 2N3790	9/12/66	P.I.		
E	CA-3429-CHG'D COMP. VALUES	5/19/67	PI		
F	CA-3749 CHG'D COMP. VALUES	5/29/67			
G	CA-3913 ADD R410 & CR401	9/14/67			

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY
H	CA-3913-1	CHG'D DIODE TYPE	10/27/67	
J	CA-4354	CHG'D TRANS TYPES & VALUES	3-29-68	

TURN OFF DELAY
TO UNREG INPUT OF -24V
SUPPLY J300-5

SIMULTANEOUS TURN OFF
TO REGULATED -24V
J300-2

J400-4
J400-1
J400-5
J400-7
J400-6
J400-2
J400-3

T2000
CR2003 MR324R
CR2004 MR324R
C2002 2000μf 50V
R2002 500Ω 10W
R402 1.5K
Q401 TN53
Q706 2N3790
R602 1.0Ω
R403 100Ω
R407 500Ω
R408 220Ω
Q402 2N703 OR 2N3391A
R404 2.2K
R412 2.2K
Q403 TN53
R413 1.2K
CR402 1/4M15Z
COMMON GRD
R416 1.78K 1%
R419 560Ω
R405 2.2K
R410 39K
C401 .47μf 75V
R409 5.6K
CR401 IN3067
Q404 2N3906
Q405 2N3906
R414 220Ω
R418 3.16K 1%
R420 1K
R411 6.8K
CR403 2N3638 *
R415 1K
R417 649Ω 1%
OUTPUT +24

*CR403 TO BE SELECTED AS PER DCS SPEC AS821001.

NOTES:
1. △ ELCO PIN CONNECTIONS TO PWR SUP MOTHER BD600
2. 2000 SERIES ARE COMPONENTS ON CHASSIS.
3. Q706 IS PART OF ASSY CA-011449
4. R602 IS PART OF ASSY BA-012093
5. REF. ASSY BA-011465
6. REF. BLOCK DIAGRAM DB-013312
7. RES. ARE AB, EB, 1/2W, 10% UNLESS OTHERWISE NOTED

REF.	DESCRIPTION	QTY

GPS-5		
PRODUCT	NEXT ASSEMBLY	QTY. ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, +24V POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN.	DH	9/23/64
CHKD	[illegible]	1/19/65
ENG.	[illegible]	2/16/67
APP.	[illegible]	2/16/67
SCALE	~	

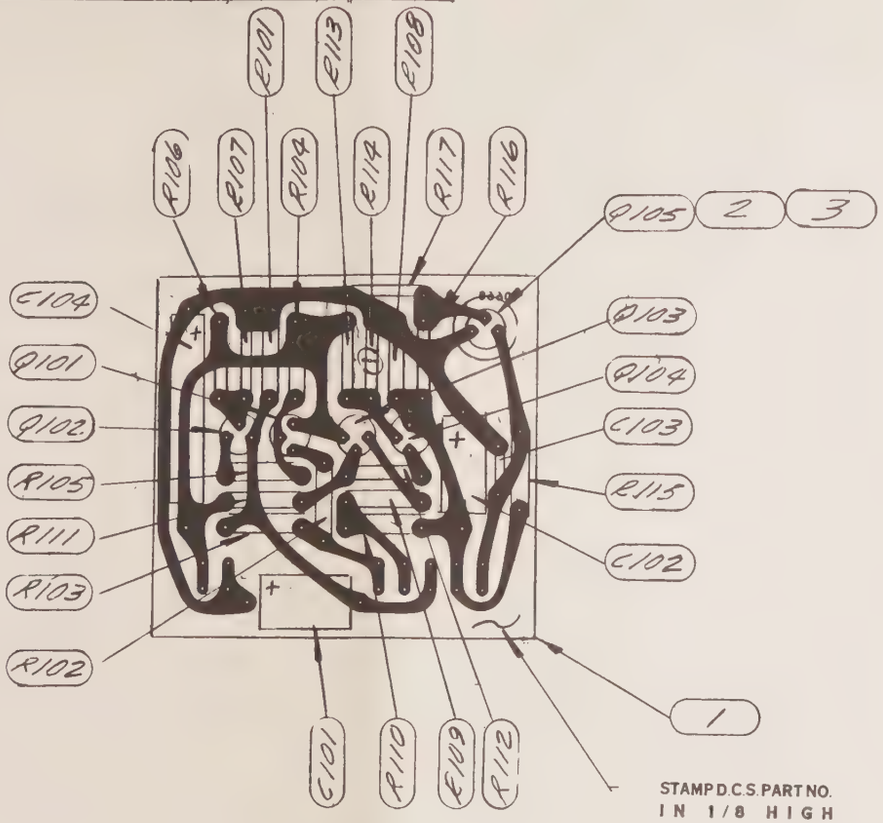
DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

BW-012743 REV. J

SHEET

BA-011471 REV J

REV.	DESCRIPTION	DATE	DWN.	CHK	APP.
C	SERIES WAS 200 R&E	3/25/64	PJH	RWG	
D	ADDED STAMP P/N NOTE R&E	7/14/64	PJH		
E	CA-2554-R106 WAS 935Ω	11/4/64			
F	CA-3190-CHG'D. COMPONENTS	3/16/66	P.I.		
G	CA-3429-CHG'D RES. VALUES	9/16/66	P.I.		
H	CA-3749 CHG COMP. VALUES	5/29/67			
J	CA-4354 CHG'D TRANS	3/29/68	DR	MR	



STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN

NOTE:

1. * PER MS 35043

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY
1		BF-010668	BOARD FAB	1
2			PAD 2055 THERMALLOY A-10068	1
3			HEAT SINK-BUF207 WAKEFIELD ENG. INC.	1
*	R101		RES, AB, EB, ½W, 10% 4.7K	1
*	R102		120Ω	1
*	R103		82Ω	1
*	R104		1K	1
*	R105		1.8K	1
*	R108		1.8K	1
*	R109		150Ω	1
*	R110		82Ω	1
*	R111		1K	1
*	R112		2.2K	1
*	R115		1K	1
	R106		RES. TI, CG ¼, ¼W, 1% 909Ω	1
	R107		1.00K	1
	R113		909Ω	1
	R114		511Ω	1
	R116		511Ω	1
	R117		464Ω	1
	C101		CAP. SPRAGUE TE 1160, 15K, 50MF	1
	C102		CAP. 15K, 50MF	1
	C103		CAP. SPRAGUE 20% SCU, 25V 0.47MF	1
	C104		CAP. SPRAGUE TE1307, 50K, 50MF	1
	Q101		TRANS. GE, 2N3391A	1
	Q102	NO SECOND CHOICE	TRANS. MOTOROLA 2N3906	1
	Q103		TRANS. GE, 2N3391A	1
	Q104	NO SECOND CHOICE	TRANS MOTOROLA 2N3906	1
	Q105		TRANS. SPRAGUE, TN5321	1

REF	DESCRIPTION	QTY

PRODUCT	NEXT ASSEMBLY	QTY/ASSY
GPS-5	DA-011452	1

DATA CONTROL SYSTEMS, INC.

TITLE: BD. ASSY. -24, -8K, -12K POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES .0, + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED √

		DATE
DWN	PJH	10/15/63
CHKD.	VJ	10/15/63
ENG.	WG	10/15/63
APP.	MJ	10/15/63
SCALE	FULL	

DO NOT SCALE DRAWING

MAT'L

FINISH

BA-011471 REV J

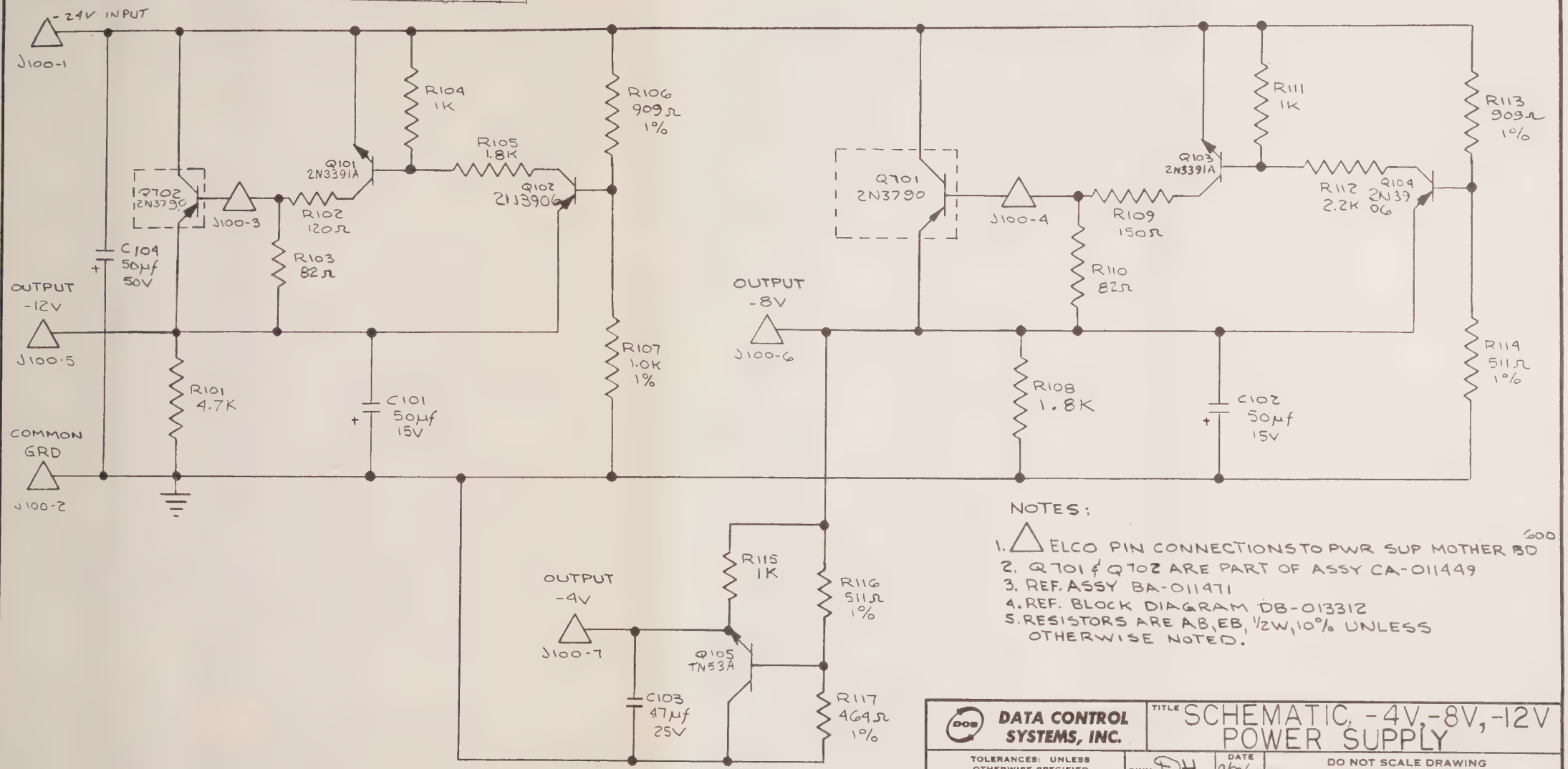
SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-2824-SYMBOL C104 WAS C204	9/14/65	RW	RWG	HM
C	CA-3190-CHG'D. COMPONENTS	3/18/66	P.I.		
D	CA-3190-2-CHG'D. Q701, &702, TO 2N3790	9/12/66	P.I		
E	CA-3429-CHG'D. RES. VALUES	9/16/66	P.I		

BW-012744 REV G

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
F	CA-3749 CHG'D COMP VALUES			5/29/68	
G	CA-4354 CHG'D TRANS TYPES VALUES			8/29/68	

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY./ASSY.



NOTES:

1. △ ELCO PIN CONNECTIONS TO PWR SUP MOTHER BD 600
2. Q701 & Q702 ARE PART OF ASSY CA-011449
3. REF. ASSY BA-011471
4. REF. BLOCK DIAGRAM DB-013312
5. RESISTORS ARE AB, EB, 1/2W, 10% UNLESS OTHERWISE NOTED.

REF.	DESCRIPTION	QTY

GPS-5		
PRODUCT	NEXT ASSEMBLY	QTY./ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE SCHEMATIC, -4V, -8V, -12V POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN. DH		9/23/69
CHKD		11/14/65
ENG.		2/14/67
APP.		2/16/67
SCALE ~		

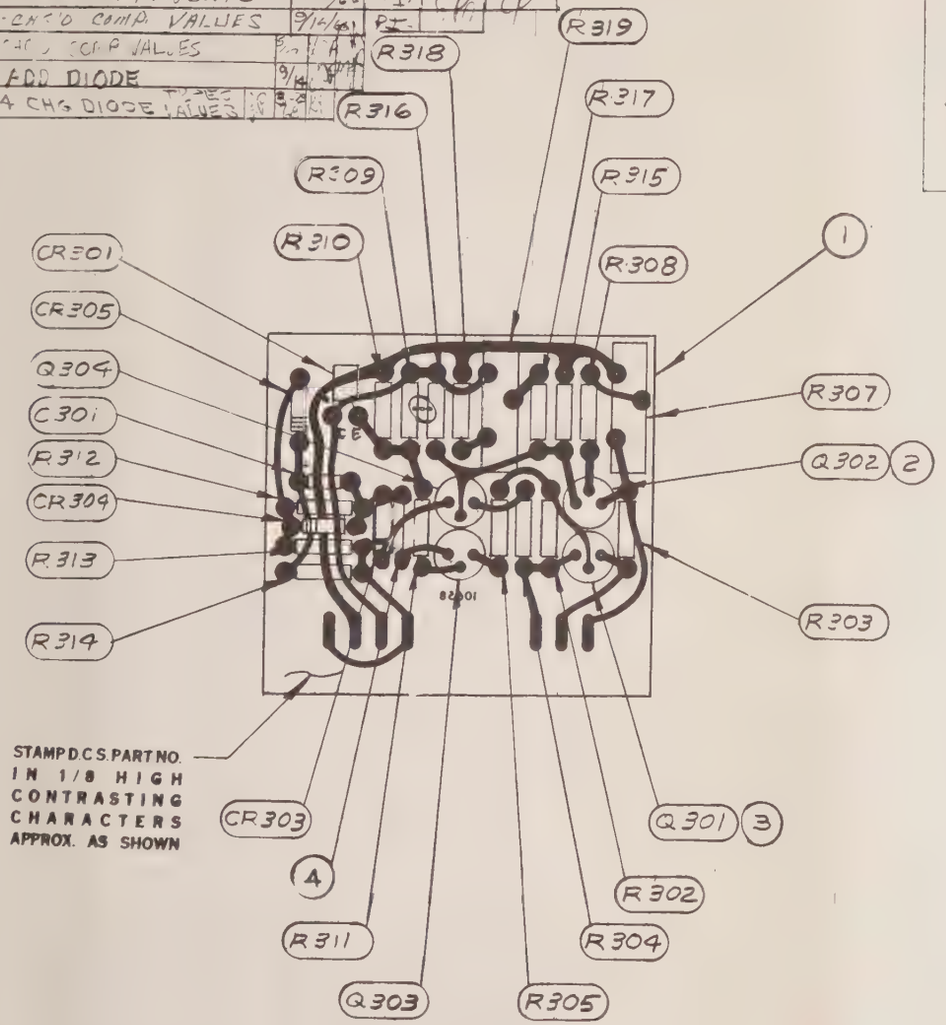
DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

BW-012744 REV. G

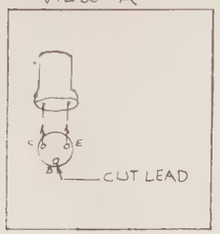
SHEET

REV	DESCRIPTION	DATE	DWN	CHK	APP
C	SERIES WAS 400 REF	3/24/64	PJH	RWC	
D	P2, 3 WERE SYL 2113 (R&E)	7/14/64	PJH		
E	CA-3190-CHG'D. COMPONENTS	3/8/66	P.I.		
F	CA-3193-CHG'D COMP. VALUES	9/14/66	P.I.		
G	CA-3193-CHG'D COMP VALUES	8/24/67			
H	CA-3913 ADD DIODE	9/14/67			
J	CA-4254 CHG DIODE TYPES & VALUES	8/2/68			

BA-011467 REV J



VIEW A



ITEM	SYMBOL	DWG NO.	DESCRIPTION	QTY/ASSY
1		BF-010658	BOARD FAB	1
2			PAD, MILTON ROSS #A10042	1
3			PAD, MILTON ROSS #A10068	1
*	R302		RES., AB, EB, 1/2W, 10%, 1K	1
*	R303		1.2Ω	1
*	R304		2.2K	1
*	R305		2.2K	1
*	R308		220Ω	1
*	R309		6.8K	1
*	R310		3.3K	1
*	R311		220Ω	1
*	R312		100K	1
*	R313		1.5K	1
*	R314		15K	1
*	R318		560Ω	1
	R319		POT, BOURNS, 3067P-1-102	1
	R315		RES., T.I., CG 1/4, 1/4W, 1%, 1.78K	1
	R316		750Ω	1
	R317		3.16K	1
	R307		POT, BOURNS, #3067-1-501 500Ω	1
	C301		CAP, SPRAGUE, 5C54, 50V, 20%, 0.47MF	1
	CR301	SEE VIEW A	DIODE, 2N3638	1
	CR303		DIODE, IN3067	1
	CR304		DIODE, MOTOROLA, 1/4M20Z	1
	CR305		DIODE, IN3067	1
	Q301		TRANS., SPRAGUE TN53	1
	Q302		TRANS., G.E., 2N3391A	1
	Q303	NO SECOND CHOICE	TRANS., MOTOROLA 2N3906	1
	Q304		TRANS.,	1
4			JUMPER #22 BUSS WIRE	1

NOTE:
1. INSTALL ITEM "2" UNDER Q302
2. INSTALL ITEM "3" UNDER Q301,
3. * PER MIL SPEC MS 35043

REF	DESCRIPTION	QTY

PRODUCT	NEXT ASSEMBLY	QTY/ASSY
GPS-5	DA-011452	1

DATA CONTROL SYSTEMS, INC.

TITLE: BD. ASS'Y, -24 V, POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ IN.
FRACTIONAL HOLES .0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN.	W.N.	10/6/63
CHKD		10/6/63
ENG.		10/6/63
APP.		10/6/63
SCALE	FULL	

DO NOT SCALE DRAWING

MAT'L

FINISH

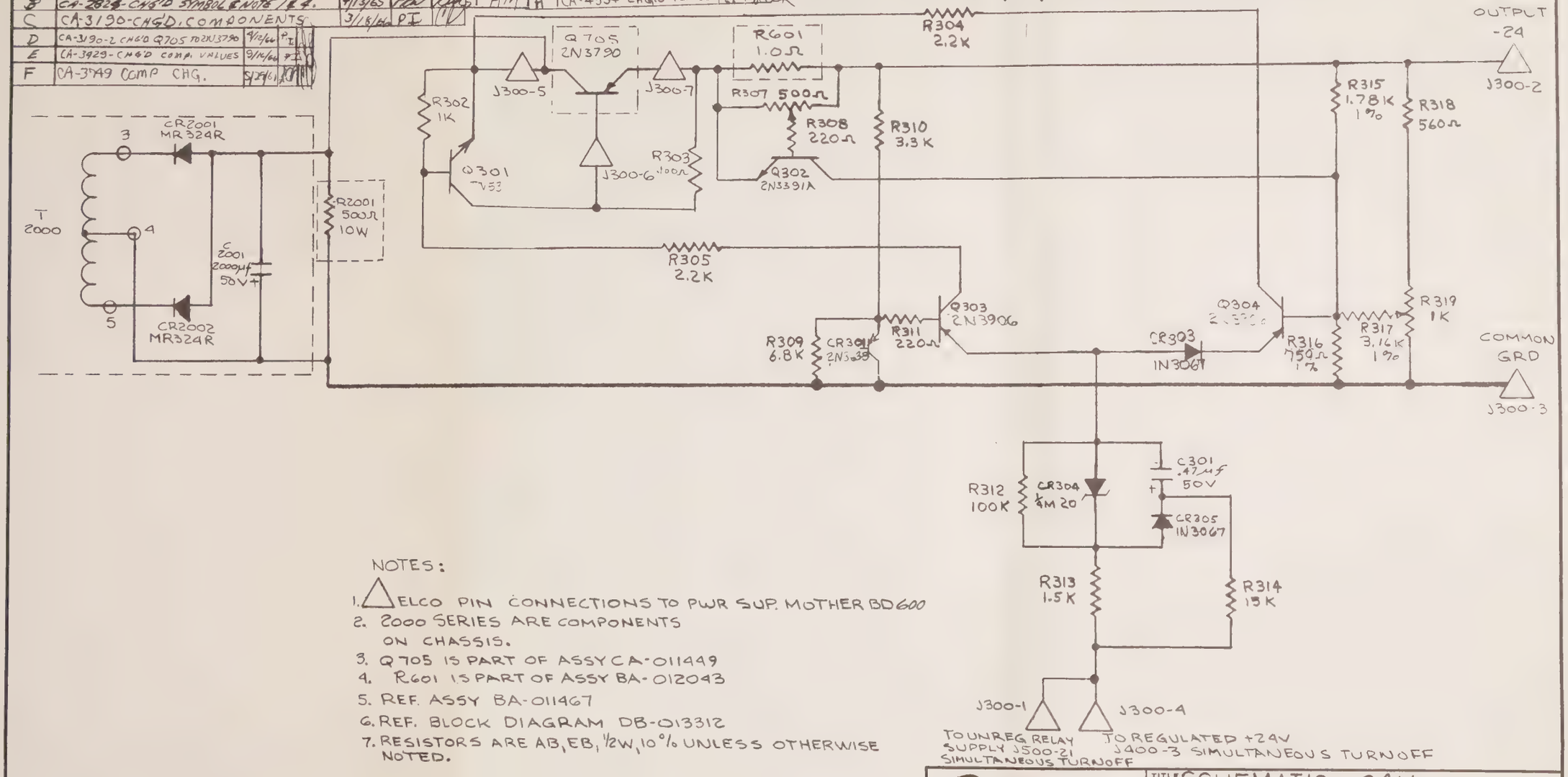
BA-011467 J

SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-2824-CHG'D SYMBOL & NOTE 1 & 4.	4/13/65			HM
C	CA-3190-CHG'D. COMPONENTS	3/16/66	PI		
D	CA-3190-2 CHG'D Q705 TO 2N3790	9/16/66	PI		
E	CA-3929-CHG'D COMP. VALUES	9/14/66	PI		
F	CA-3949 COMP CHG.	5/25/67			
G	CA-3913 MDR CR303	8/4/67			
H	CA-4354 CHG'D TRANS	3-29-68			

BW-012735 REV H

...M	SYMBOL	DWG. NO.	DESCRIPTION	QTY / ASSY



NOTES:

1. △ ELCO PIN CONNECTIONS TO PWR SUP. MOTHER BD600
2. 2000 SERIES ARE COMPONENTS ON CHASSIS.
3. Q705 IS PART OF ASSY CA-011449
4. R601 IS PART OF ASSY BA-012043
5. REF. ASSY BA-011467
6. REF. BLOCK DIAGRAM DB-013312
7. RESISTORS ARE AB, EB, ½W, 10% UNLESS OTHERWISE NOTED.

REF.	DESCRIPTION	QTY

GPS-5		
PRODUCT	NEXT ASSEMBLY	QTY. / ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE SCHEMATIC -24V POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ✓

		DATE
DWN.	R.C.	9/28/64
CHKD.		1/19/65
ENG.		2/16/65
APP.		2/16/65
SCALE	~	

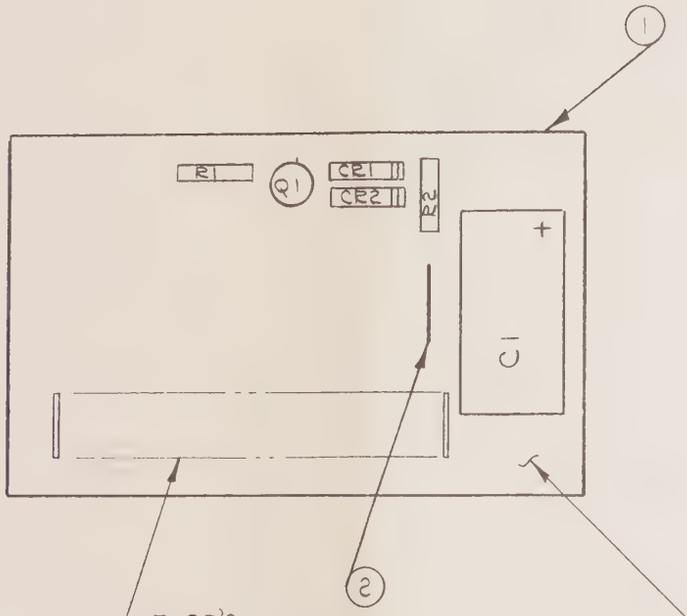
DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

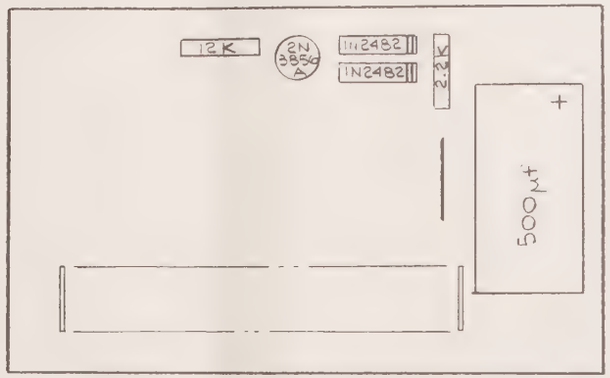
BW-012735 REV H

SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B					

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY / ASSY
1		BF-010677	BD FAB.	1
2			JUMPER #22 BUSS	AR
	R1		RES., AB EB, 1/2W, 10% 2K	1
	R2		RES, AB EB, 1/2W, 10% 2.2K	1
	Q1		TRANS, G.E. 2N3854A	1
	C1		CAP, SPRAGUE, TA-3.5 35V, 2500MF	1
	CR1		DIODE, SARKES TARZIAN 1N2482	1
	CR2		" 1N2482	1





500 SERIES

STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN

REF.	DESCRIPTION	QTY

PRODUCT	NEXT ASSEMBLY	QTY. / ASSY.
GPD-6	BA-015319	1

DATA CONTROL SYSTEMS, INC.

TITLE: INDICATOR LITES POWER SUPPLY BD.

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN. GB	B	8/24/66
CHKD. RW		8/25/66
ENG. [illegible]		8/26/66
APP. PAV		8/29/66
SCALE —		

DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

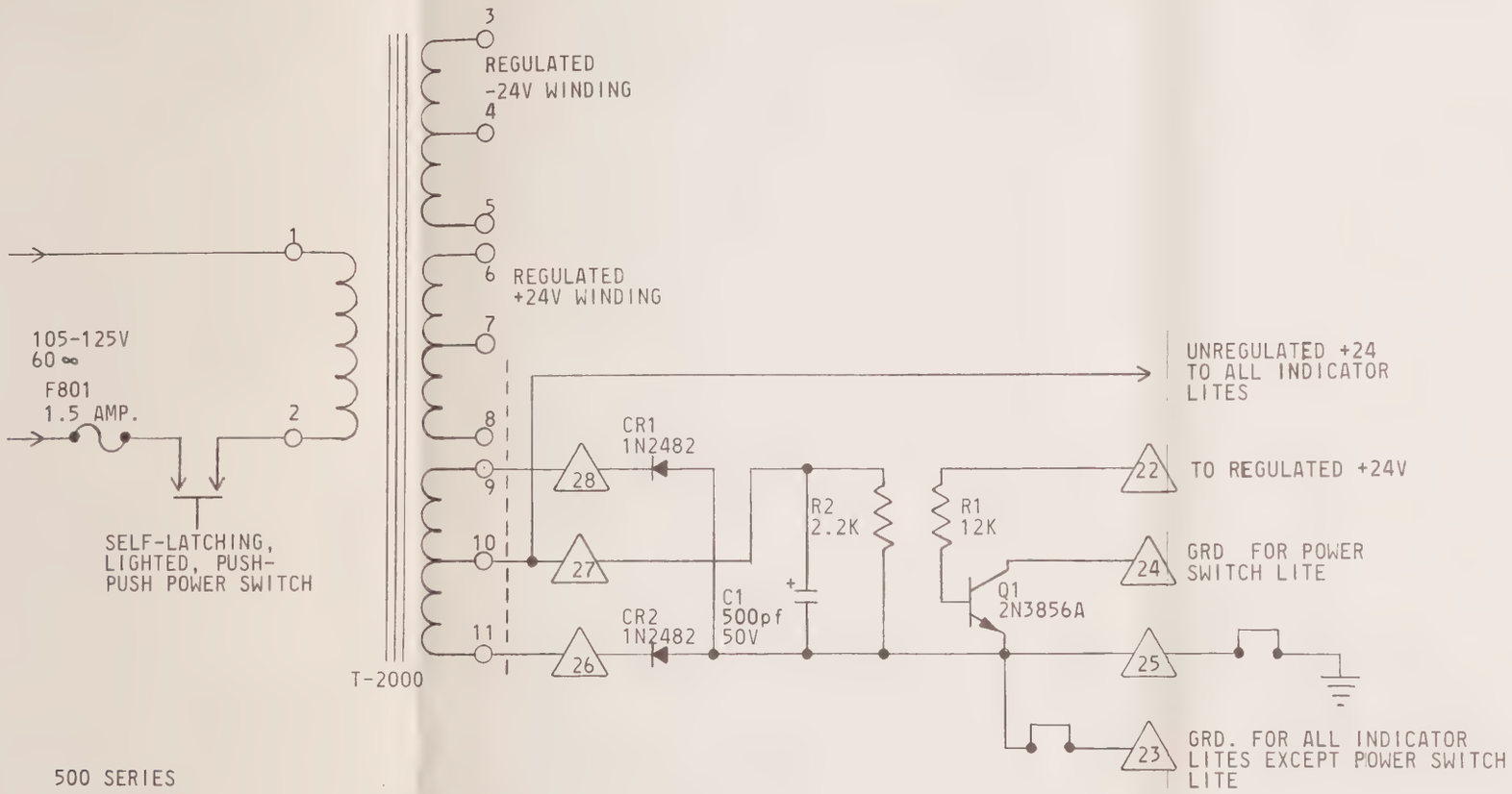
BA-015197 REV. A

SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.

B

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY



NOTES: 500 SERIES

1, Δ ELCO PIN CONNECTIONS J500 TO POWER SUPPLY MOTHER BOARD 600.
2, REF. ASSY - BA-015197.
3, REF. BLOCK DIAGRAM BB-015326
4, RES. ARE AB,EB, 1/2W, 10%

REF.	DESCRIPTION	QTY

GPD-6

PRODUCT	NEXT ASSEMBLY	QTY. ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, INDICATOR LITES POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN —— /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED

		DATE
DWN.	W.B.	8/26/66
CHKD.		
ENG.		
APP.		
SCALE	~	

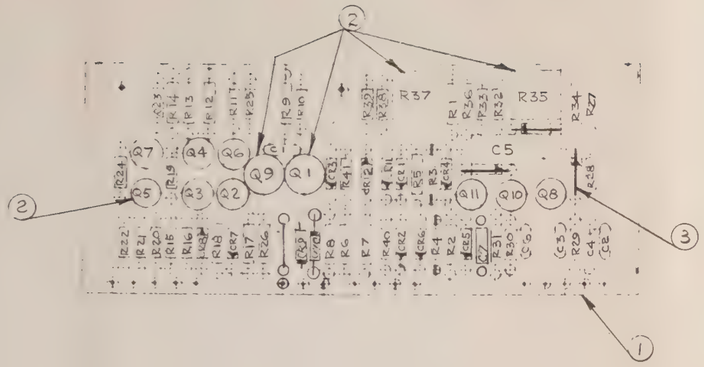
DO NOT SCALE DRAWING

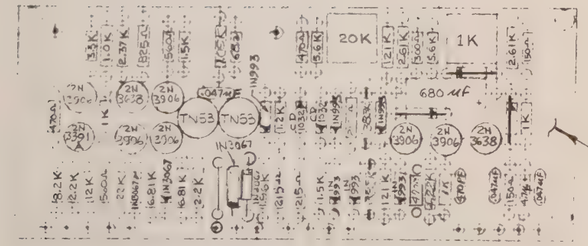
MAT'L ~

FINISH ~

BW-015277 REV. A

SHEET





STAMP D C S PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN

Ø COMPARATOR BD.

1700 SERIES

Ø COMP BD

ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
	R1	121K	ELECTRA MF5C-D 1%, 1/4W	
	R2	121K	ELECTRA MF5C-D 1%, 1/4W	
	R3	383K	ELECTRA, MF5C, 1/4W 1%	
	R4			
	R5	215Ω	ELECTRA, MF5C-D 1%, 1/4W	
	R6	215Ω		
	R7	215Ω		
	R8	1.96K	MF6C-D 1/2W	
	R9	1.05K	ELECTRA, MF5C-D 1/4W, 1%	
	R10	68Ω	AB, CB 10% 1/4W	
	R11	560Ω	AB, CB 10%	
	R12	825Ω	ELECTRA MF5C-D 1%, 1/4W	
	R13	2.37K		
	R14	10K		
	R15	560Ω	AB, CB 10% 1/4W	
	R16	22K	AB, CB 10%	
	R17	6.81K	ELECTRA MF5C-D 1%, 1/4W	
	R18	6.81K	ELECTRA MF5C-D 1%, 1/4W	
	R19	1K	AB, CB 10%, 1/4W	
	R20	12K		
	R21	2.4K		
	R22	8.2K		
	R23	3.3K		
	R24	470Ω		
	R25	1.5K		
	R26	2.2K	AB, CB 10%, 1/2W	
	R27	150Ω	AB, CB 10%, 1/4W	
	R28	1K		
	R29	150Ω		
	R30	1K		
	R31	4.22K	ELECTRA, MF5C-D 1%, 1/4W	
	R32	5.6K	AB, CB 5%, 1/4W	
	R33	300Ω	AB, CB 5%,	
	R34	2.61K	ELECTRA MF5C-D 1%, 1/4W	
	R35	1K	IRC CIRCUITRON 201-10, 1K	
	R36	2.61K	ELECTRA MF5C-D 1%, 1/4W	

Ø COMP BD

ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
	R37	20K	IRC CIRCUITRON 201-10, 20K	
	R38	5.6K	AB, CB 10% 1/4W	
	R39	470Ω		
	R40	1.5K		
	R41	1.2K		
	C1	.047MF	SPRAGUE 3C15 25V 20%	
	C2	.047MF		
	C3	.047MF		
	C4	4.7MF	SPRAGUE 150D 10% 10V	
	C5	680MF	SEMCOR TSN3K-687,3V	
	C6	470PF	ERIE, 831-000-X5F0-471K, 10%	
	C7	470 pf	DURMICA 10%	
	C8	1-10 pf F.A.	DURMICA 1% ACROSS R3 OR R4	
	CR1	IN993		
	CR2	IN993		
	CR3	IN993		
	CR4	IN993		
	CR5	IN993		
	CR6	IN993		
	CR7	IN3067		
	CR8	IN3067		
	CR9	IN3067	SEE NOTE 1	
	CR10	IN3067	SEE NOTE 1	
	IC11	CD1032	CONT. DEVICES	
	IC12	CD1032		

Ø COMP. BOARD

ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
	Q1	TN53	SPRAGUE, 2ND CHOICE 2N2218	
	Q2	2N3906		
	Q3	2N3906		
	Q4	2N3638		
	Q5	2N3391A		
	Q6	2N3906		
	Q7	2N3906		
	Q8	2N3638		
	Q9	TN53	SPRAGUE, 2ND CHOICE 2N2218	
	Q10	2N3906		
	Q11	2N3906		
1		CF-014988	BD. FAB COMP BD.	1
2			TRANS PADS, ROSS #A10068	4
3			JUMPER #22 BUSS	A/R

1700 SERIES

SHEET 3 OF 3

REVISIONS					
S.M.	DESCRIPTION	DATE	BY	CHK'D	APP'D
B	(RHE) 2N4250 WAS 2N3906 REMOVED CR9 & CR10	3/1/67	RTW		
C	CA-3750 CHG'D COMP. POSITIONS & VALUES	6/1/67	[illegible]	[illegible]	[illegible]
D	CA-3850 CHG'D CAP. STYLE	7/11/67	[illegible]	[illegible]	[illegible]
E	CA-3982 ADD NOTE #1	11/1/67	[illegible]	[illegible]	[illegible]
F	CA-4413 CHG'D R8 TYPE	4-19-68	[illegible]	[illegible]	[illegible]

NOTES:
*1) -1 DESIGNATES THE USE OF CR-9 & CR-10
-2 " OMISSION OF CR-9 AND THE REPLACEMENT OF CR-10 WITH A #22 BUSS JUMP
2) -1 INDICATES GPS-5 & 6
-2 INDICATES GPD-6

DATA CONTROL SYSTEMS, INC.

TITLE: PHASE COMPARATOR BOARD ASSEMBLY, GPD-6, GPS-5 & 6

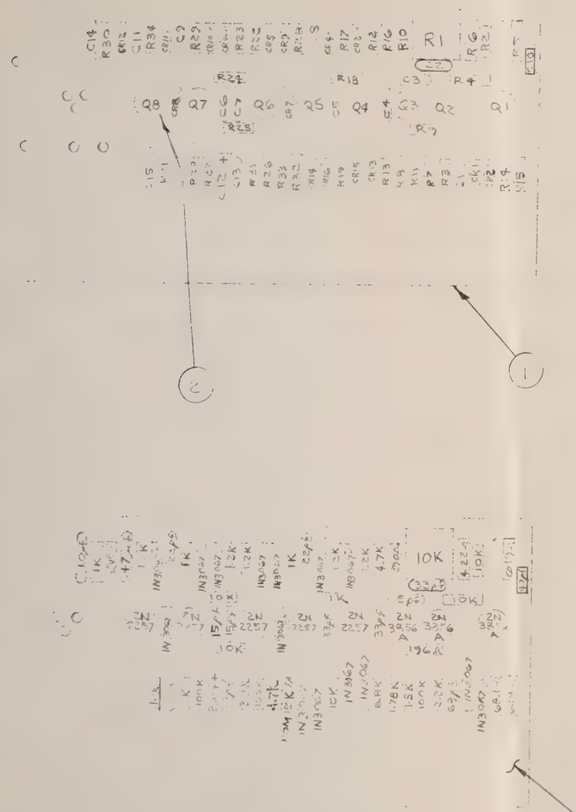
TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC ± 1/64 ANG ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE BREAK ALL SHARP CORNERS .005"-.015"

DO NOT SCALE DRAWING

DWN J. WALKER DATE 6-30-66
CHK'D RTW 9/25/66
PROG ENG
CH ENG
SCALE NONE

MAT -
FINISH

GA-015155 * REV F



METER B.D. LESS 2f DRIVER
1400 SERIES

STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY REQ'D
	R1	10K	IRC POT 201-10-10K	1
	R2	10K	AB,CB, 10% 1/4W	1
	R3	2.2K	AB,CB, 10% 1/4W	1
	R4	10K	ELECTRA, MF5C-D, 1% 1/4W	1
	R5	619Ω		1
	R6	422Ω		1
	R7	100K		1
	R8	1.78K		1
	R9	196Ω		1
	R10	390Ω	AB,CB, 10% 1/4W	1
	R11	1.8K		1
	R12	1.2K		1
	R13	6.8K		1
	R14	68.1Ω	ELECTRA, MF5C-D, 1%	1
	R15	619Ω	ELECTRA, MF5C-D, 1%	1
	R16	4.7K	AB,CB, 10% 1/4W	1
	R17	1.2K		1
	R18	1K		1
	R19	10K		1
	R20	1K		1
	R21	10K		1
	R22	1.2K		1
	R23	1.2K		1
	R24	10K		1
	R25	10K		1
	R26	100K		1
	R27	100K		1
	R28	1K		1
	R29	1K		1
	R30	1K	AB,EB, 10%, 1/2W	1
	R31	3.9K	AB,CB, 10% 1/4W	1
	R32	15K NOM.F.A.		1
	R33	4.7K	AB,CB, 10% 1/4W	1
	R34	1.2K	AB,CB, 10% 1/4W	1

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY REQ'D
	C1	68pf	ERIE, 831-[illegible]	1
	C2	33pf	ERIE, 831-[illegible]	1
	C3	5pf	ERIE, 831-[illegible]	1
	C4	33pf	ERIE, 831-[illegible]	1
	C5	33pf	ERIE, 831-[illegible]	1
	C6	15pf	ERIE, 831-U2M-150X, 10%	1
	C7	15pf	ERIE, 831-U2M-150X, 10%	1
	C8	22pf	ERIE, 831-[illegible]	1
	C9	22pf	ERIE, 831-[illegible]	1
	C10	47pf	ERIE, 831-[illegible]	1
	C11	.47uf	SPRAGUE, 5C11, 25V	1
	C12	22uf	SPRAGUE, 150D, 15V, 20%	1
	C13	33pf	ERIE, 831-[illegible]	1
	C14	1.0uf	SPRAGUE, 5C13, 25V	1
	C15	1.0uf	SPRAGUE, 5C13, 25V	1
1		CF-015059	BD. FAB, METER	1
2			TRANS PADS, THERMALLOY, 7717-7N	5

1400 SERIES

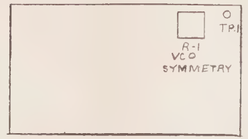
ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY REQ'D
	CR1	1N3067	CONTINENTAL DEVICES	1
	CR2	1N3067		1
	CR3	1N3067		1
	CR4	1N3067		1
	CR5	1N3067		1
	CR6	1N3067		1
	CR7	1N3067		1
	CR8	1N3067		1
	CR9	1N3067		1
	CR10	1N3067		1
	CR11	1N3067		1
	CR12	SV5	TRANSITRON	1
	CR13	1N3067	CONTINENTAL DEVICES	1
	CR14	1N3067		1
	CR15	1N3067		1
	CR16	1N3067		1
	Q1	2N3856A	G.E.	1
	Q2	2N3856A		1
	Q3	2N3856A		1
	Q4	2N2257	MOTOROLA	1
	Q5	2N2257		1
	Q6	2N2257		1
	Q7	2N2257		1
	Q8	2N2257		1

REVISIONS					
SYM.	DESCRIPTION	DATE	BY	CHK'D	APP'D
B	CA-3850 CHGD CAP TYPES	7/11/67	JCD	CLC	EGC
C	PA 413 CHG PSE 1 - 2 & E32 A 9-68				ER

WITHOUT $2F_c$ DRIVER

DATA CONTROL SYSTEMS, INC.	TITLE: METER BD ASS'Y	
TOLERANCES UNLESS OTHERWISE SPECIFIED DECIMAL - 3 PLACE ± .005 DECIMAL - 2 PLACE ± .010 FRAC. ± 1/64 ANG. ± 0°30' FLATNESS WITHIN /IN. FRACTIONAL HOLES -0, + 1/64 NOTE: BREAK ALL SHARP CORNERS .005"-.015"	DWN RE 8/29/66 CHKD TW PROJ ENG 8/29/66 CH ENG SCALE ~	DO NOT SCALE DRAWING GPD-6 E-215 GA-015322 REV C

REV.	DESCRIPTION	DATE	DWN	CHK.	APP.
B	CA-4413 CHG'D R33 VALUE	4-19-68	JR.		



SKETCH SHOWING LOCATION OF TEST POINT

NOTES:
1. △ ELCO PIN CONNECTIONS TO MOTHER BD
2. REF. ASSY. GA-015322
3. REF. BLOCK DIAGRAM DB-015327
4. ALL RESISTORS ARE AB, CB, 1/4W, 10 % UNLESS OTHERWISE NOTED.

2 FC GENERATOR DRIVER

NOTE:
THESE COMPONENTS ARE OMMITED EXCEPT ON SPECIAL ORDERS REQUIRING THE USE OF AN EXTERNAL COHERENT CLOCK DIVIDER.

VCO SYMMETRY ○ TP-1

J-2 +12V

VCO SYMMETRY R-1 10K

R-2 10K

R-3 2.2K

R-4 10K 1%

R-5 619Ω 1%

R-6 422Ω 1%

C-2 33pf

C-3 5μμf

R-9 196Ω 1%

47μ C 10

Q-1 2N3856-A

Q-2 2N3856A

CR-1 IN3067

CR-2 IN 3067

J-14 INPUT FROM V.C.O. AMP. ON Ø COMP BD BD 1700

+3 -3

J-3 +8

R37 1.2K

R38 100Ω

C18 22 mf 20V

Q-9 2N3638

J-9 INPUT

R-35 4.7K

C16 10mf 20V

C17 10mf 20V

R36 2.7K

CR17 IN3067

CR18 IN3067

R39 1K

C19 10mf 20V

CR19 IN3067

CR20 IN3067

J-8 OUTPUT

R-14 68.1Ω 1%

R-15 619Ω 1%

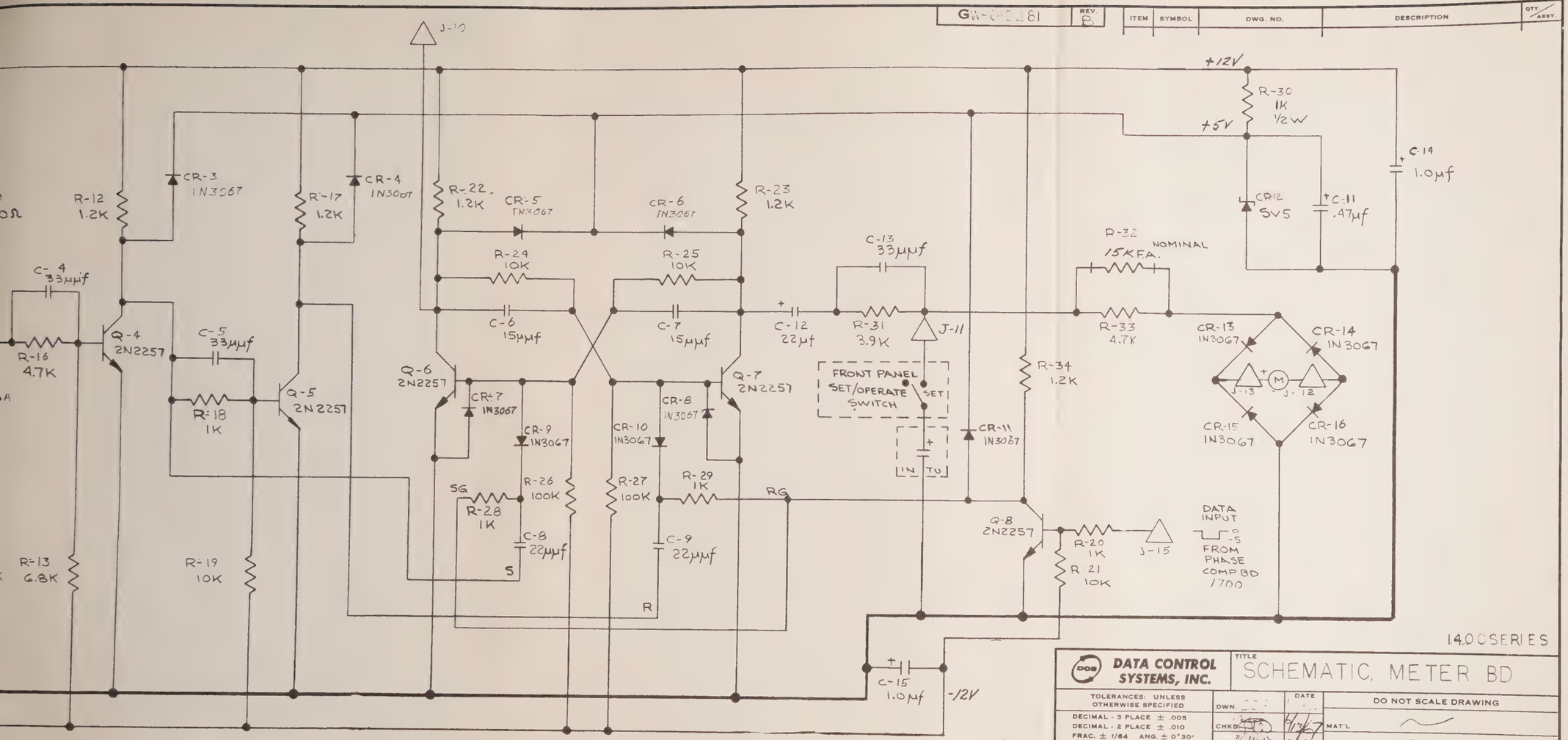
R-7 100K 1%

R-8 1.78K 1%

J-7 GRD.

J-5 -12V

REF.	DESCRIPTION	QTY



GW-015281 REV. B

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY./ASSY.

1400 SERIES

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, METER BD

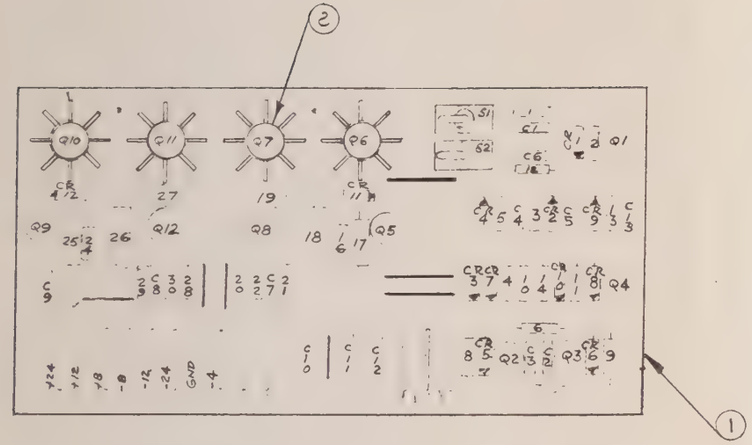
TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED

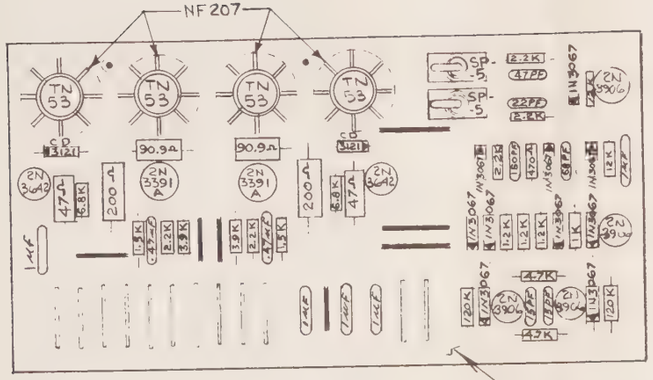
	DATE
DWN.	
CHKD.	4/17/67
ENG.	6/3/67
APP.	4/19/67
SCALE	

DO NOT SCALE DRAWING
MAT'L
FINISH
GW-015281 REV. B
SHEET

GPD-6

FIRST PRODUCT	NEXT ASSEMBLY	QTY./ASSY.





	R1	2.05K	AB, CE, ...
	R2	12K	
	R3	470Ω	
	R4	1.2K	
	R5	2.2K	
	R6	4.7K	
	R7	4.7K	
	R8	120K	
	R9	12K	
	R10	1.2K	
	R11	1K	
	R12	2.2K	
	R13	12K	
	R14	1.2K	▼
	R16	6.8K	R2, CR3, ...
	R17	47Ω	R3, CR3, ...
	R18	200Ω	MEPCO, ...
	R19	90.9Ω	MEPCO, P...
	R20	3.9K	R3, CR3, ...
	R21	1.5K	
	R22	2.2K	▼
	R24	6.8K	R3, CR3, ...
	R25	47Ω	R3, CR3, ...
	R26	200Ω	MEPCO, ...
	R27	90.9Ω	MEPCO, P...
	R28	3.9K	R3, CR3, ...
	R29	1.5K	
	R30	2.2K	▼
ITEM	SYMBOL	PART NO.	DES...

1500 SERIES

NRZ CODE CONVERTER
+ LINE DRIVERS

1500 SERIES

GPD-6

ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
	C1	47 pF	ERIE, 831-006-XFO-470K	
	C2	15 pF	831-000-X5FO-151K ..	
	C3	15 pF		
	C4	150 pF		
	C5	68 pF	831 10% X5R-680K	
	C6	82 pF	831 000-U2J0-220J	
	C7	.47 MF	SPRAGUE, 5C11, 25V	
	C8	.47 MF	SPRAGUE, 5C11, 25V	
	C9	1 MF	SPRAGUE, 5C13, 15V	
	C10	1 MF		
	C11	1 MF		
	C12	1 MF		
	C13	1 MF		
	CR1	IN3067		
	CR2	IN3067		
	CR3	IN3067		
	CR4	IN3067		
	CR5	IN3067		
	CR6	IN3067		
	CR7	IN3067		
	CR8	IN3067		
	CR9	IN3067		
	CR10	IN3067		
	CR11	CD3121	CONT. DIVICES	
	CR12	CD3121		

SHEET 2 OF 3

GPD-6

ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
	Q1	2N3640	MOTOROLA NO SECOND CHOICE	
	Q2			
	Q3			
	Q4			
	Q5	2N3642		
	Q6	TN53	SPRAGUE, 2ND CHOICE, 2N2218	
	Q7	TN53		
	Q8	UNI339A		
	Q9	2N3642		
	Q10	TN53	SPRAGUE, 2ND CHOICE, 2N2218	
	Q11	TN53		
	Q12	UNI339A		
	S1	TOKEHL SWITCH	STD-5 TOG, BUSH 5	
	S2	TOKEHL SWITCH	STD-5 TOG, SH SHANKE	
	4	HEAT SINKS	NF-207 WAKEFIELD ENG.	
	4	JUMPERS .40 LONG		
	3	JUMPERS .60 LONG		
1		CF-014953	BD. FAB, NRZ CODE CONVERTER	1
2			TRANS PADS, ROSS #A10068	6

SHEET 3 OF 3

REVISIONS					
SYM	DESCRIPTION	DATE	BY	CHK'D	APP'D
B	(RYE) 2N4250 NAS 2N3906	2/3/67	RTW		
C	CA-3850 CHG'D CAP STYLE →	7/[illegible]/67	[illegible]		
D	CA-4354 CHG'D TR[illegible] T[illegible]	3/[illegible]	[illegible]		

DATA CONTROL SYSTEMS, INC.

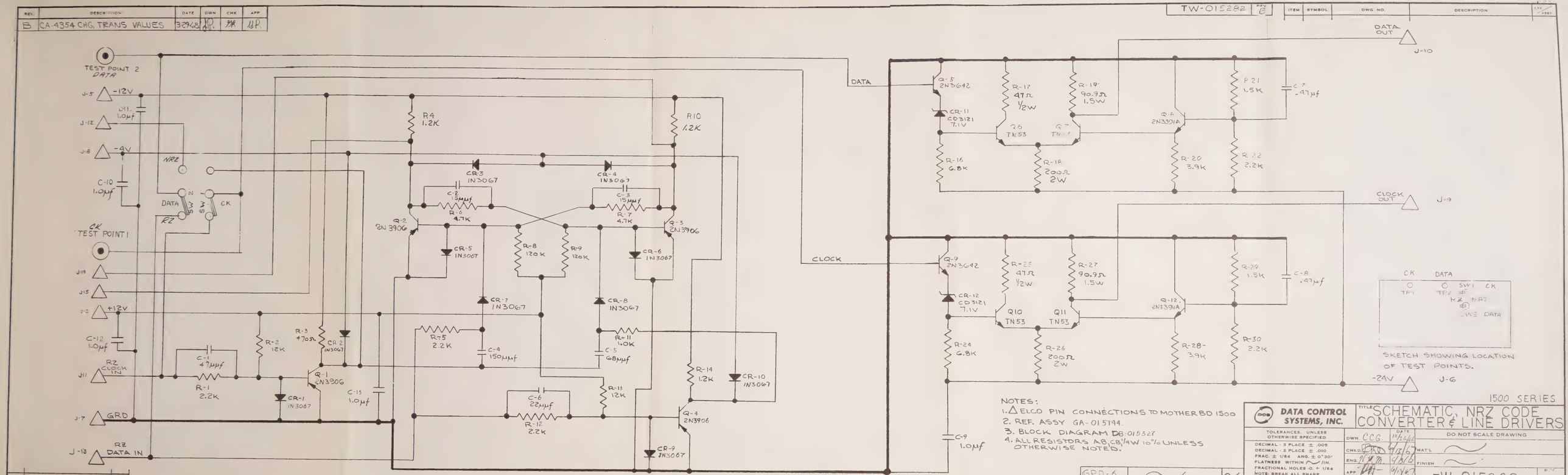
TITLE: NRZ CODE CONVERTER + LINE DRIVERS, GPD-6

TOLERANCES: UNLESS OTHERWISE SPECIFIED	J. WALKER	DATE 6-28-66	DO NOT SCALE DRAWING
DECIMAL - 3 PLACE ± .005	DWN.		
DECIMAL - 2 PLACE ± .010	CHK'D RTW	9/25/66	MAT'L
FRAC. ± 1/64 ANG. ± 0°30'	PROJ. ENG.		
FLATNESS WITHIN /IN.	CH. ENG.	9/26/66	FINISH
FRACTIONAL HOLES -0, + 1/64	SCALE NONE		
NOTE: BREAK ALL SHARP CORNERS .005"-.015"			GA-015144 REV. D

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-4354 CHG. TRANS. VALUES	3/9/68	[illegible]	[illegible]	[illegible]

TW-015282 REV B

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY / ASSY



SKETCH SHOWING LOCATION OF TEST POINTS.

NOTES:
1. △ ELCO PIN CONNECTIONS TO MOTHER BD 1500
2. REF. ASSY GA-015194
3. BLOCK DIAGRAM DB-015328
4. ALL RESISTORS AB, CB, 1/4W 10% UNLESS OTHERWISE NOTED.

REF.	DESCRIPTION	QTY

1500 SERIES

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, NRZ CODE CONVERTER & LINE DRIVERS

TOLERANCES, UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /in.
FRACTIONAL HOLES Ø + 1/64
NOTE- BREAK ALL SHARP CORNERS .005" - .015"
SURFACE ROUGHNESS NOT TO EXCEED ~

DO NOT SCALE DRAWING

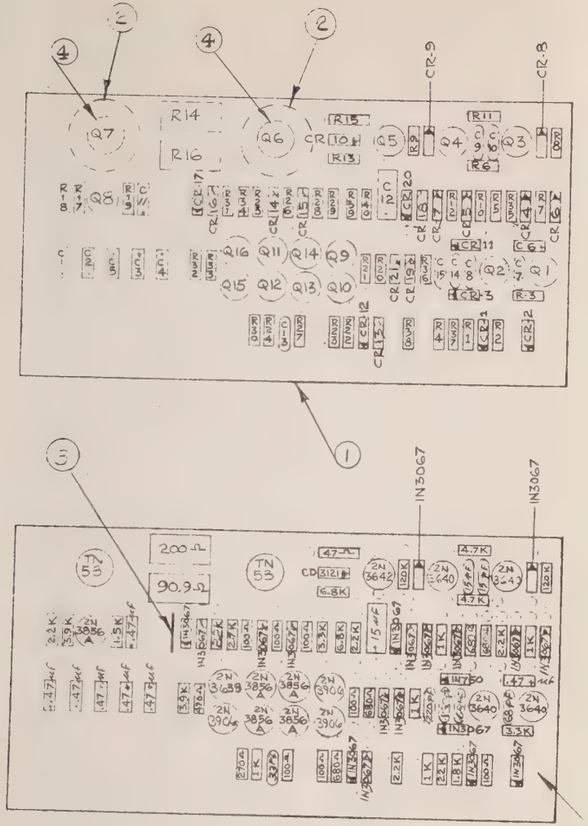
		DATE
DWN.	CCG.	10/24/67
CHK'D.	[illegible]	9/26/67
ENG.	[illegible]	9/26/67
APP.	[illegible]	9/26/67
SCALE	~	

MAT'L ~
FINISH ~

GPD-6 | FIRST PRODUCT | NEXT ASSEMBLY | QTY / ASSY ~

TW-015282 REV B

SHEET



SYNCHRO DET. BD.
1800 SERIES

STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN

SYNCHRO. DET. BD.

	R1	1.8K	AB, CB, 10%, ¼W		
	R2	100Ω			
	R3	9.3K			
	R4	1K			
	R5	680Ω			
	R6	4.7K			
	R7	1K			
	R8	120K			
	R9	120K			
	R10	680Ω			
	R11	4.7K			
	R12	1K			
	R13	6.8K			
	R14	200Ω	MEPCO, P120 5%, 2½W		
	R15	47Ω	AB, EB, 10% ← ½W		
	R16	90.9Ω	MEPCO, P120 1%, 2½W		
	R17	3.9K	AB, CB, 10%, ¼W		
	R18	2.2K			
	R19	1.5K			
	R20	680Ω			
	R21	100Ω			
	R22	680Ω			
	R23	100Ω			
	R24	1K			
	R25	100Ω			
	R26	100Ω			
	R27	100Ω			
	R28	100Ω			
	R29	3.3K			
	R30	270Ω			
	R31	2.2K			
	R32	3.9K			
	R33	470Ω			
	C24	2.7K			
	R35	2.2K			
	R36	1K			
ITEM	SYMBOL	PART NO.	DESCRIPTION		QTY REQ'D

1800 SERIES

	R37	3.3K	R3-5 2%, ¼W		
	R38	2.2K			
	R39	6.8K			
	R40	3.3K			
	CR1	IN3067			
	CR2	IN3067			
	CR3	IN3067			
	CR4	IN3067			
	CR5	IN3067			
	CR6	IN3067			
	CR7	IN3067			
	CR8	IN3067			
	CR9	IN3067			
	CR10	CD312	CONT DEVICES		
	CR11	N750			
	CR12	1N3064			
	CR13	N3067			
	CR14	IN3067			
	CR15	IN3067			
	CR16	IN3067			
	CR17	IN3067			
	CR18	IN3067			
	CR19	IN3067			
	CR20	IN3067			
	CR21	IN3067			
1		CF-015003	BD. FAB, SYNCHRO DET		1
2			HEAT SINK WAKEFIELD #NF-207		2
3			JUMPER #24 BLK. INSULATED WIRE		4/R
4			TRANS PADS, ROSS #A10068		2
ITEM	SYMBOL	PART NO.	DESCRIPTION		QTY REQ'D

GPD-6
SYNCHRO. DET, 3D

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY. REQ'D
	Q1	2N3640		
	Q2	2N3640		
	Q3	2N3640		
	Q4	2N3640		
	Q5	2N3642		
	Q6	TN53	SPRAGUE, 2ND CHOICE 2N2218	
	Q7	TN53	↓	
	Q8	2N3856A		
	Q9	2N3906	MOTOROLA, NO SECOND CHOICE	
	Q10	2N3906	↓ ↓	
	Q11	2N3856A		
	Q12	2N3856A		
	Q13	2N3856A		
	Q14	2N3856A		
	Q15	2N3906	MOTOROLA, NO SECOND CHOICE	
	Q16	2N3638		
	C1	.47MF	SPRAGUE, 150D 35V 20%	
	C2	.47MF	↓ ↓	
	C3	.47MF		
	C4	.47MF		
	C5	.47MF		
	C6	.47MF		
	C7	68PF	ET [illegible] 82 [illegible] 15% X5R-680K	
	C8	68PF	X5R-680K	
	C9	15PF	↓ ↓ U2M-150K	
	C10	15PF	↓ ↓ ↓ U2M-150K	
	C11	.47MF	SPRAGUE, 150D 35V 20%	
	C12	15MF	↓ 150D 20V 20%	
	C13	33PF	CAP, ERIE 831-000-U2J0-330J	
	C14	150PF	831-000-X5F0-151K	
	C15	220PF	831-000-X5F0-221J	

SHEET 3 OF 3

REVISIONS					
LTR	DESCRIPTION	DATE	BY	CHK'D	APP'D
B	[RVE] 2N4250 WAS 2N3906	3/3/67	RTW		
C	CA-3750 CHG'D COMP. VALUES	6/1/67	[illegible]	6-7-67	[illegible]
D	CA-3850 CHGD CAP STYLE	9/11/67	[illegible]	[illegible]	[illegible]
E	CA-3750-1 ADD 2 & 3	9/13/67	[illegible]	[illegible]	[illegible]
F	CA-4354 CHG'D TRANS TYPES & VALUES	3-29-68	AP	GR	GR
G	CA-4413 CHG'D C14 VALUE & TYPE	4-19-68	AP	GR	GR

1800 SERIES

DATA CONTROL SYSTEMS, INC.

TITLE: SYNCHRO, DET. BOARD ASSEMBLY GPD-6

UNLESS OTHERWISE SPECIFIED: DECIMAL ± .010, FRACTIONAL ± 1/64, SURFACES WITHIN ~ IN, FRACTIONAL HOLES ± 1/64, REMOVE BURRS & SHARP CORNERS

		DATE
DRAWN	J. WALKER	6-29-66
CHECKED	RTW	8/26/66
ENG.	[illegible]	8/26/66
APPD.	[illegible]	8/26/66

SCALE: NONE

DO NOT SCALE DRAWING

MATL ~

FINISH ~

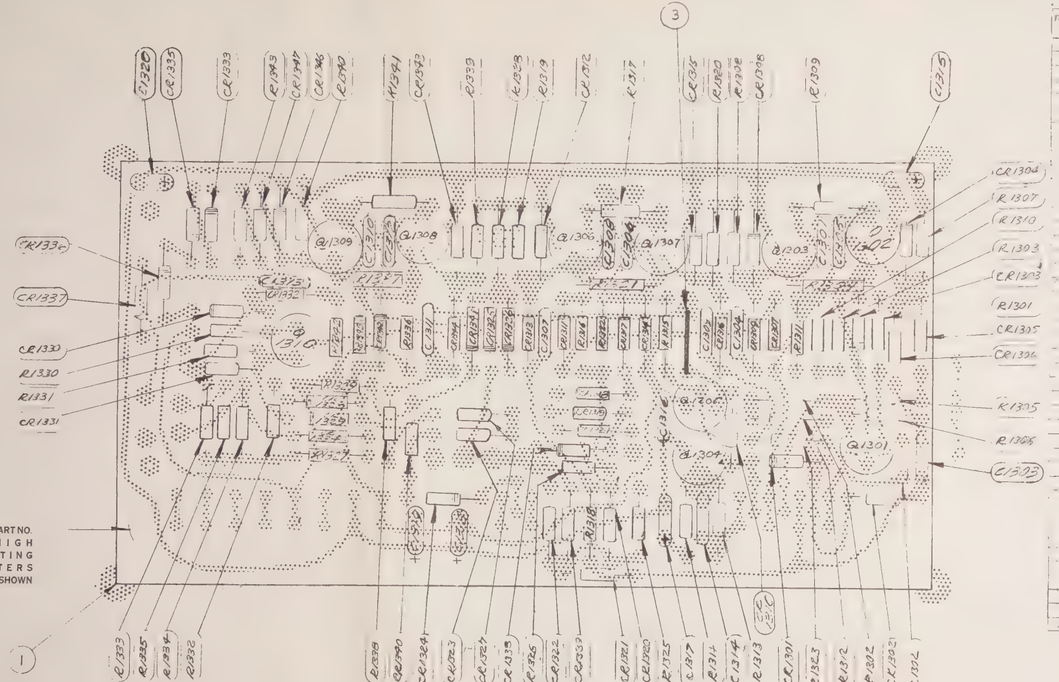
GA-015151

REV. G

REV	DESCRIPTION	DATE	DWN	CHK	APP
B	CA-2621 CHG VALUES	12/6/63	DH	[illegible]	[illegible]
C	CA-3190-CHG'D VALUE OF R1312	5/18/64	PD	[illegible]	[illegible]
D	CA-3-10-1 - ADD JUMPER	7/24/64	PE	[illegible]	[illegible]
E	CA-3749 CHG COMP VALUES	8/31/64	[illegible]	[illegible]	[illegible]
F	CA-3849 CHG CAP VALUES	9/11/64	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
H	CA-3849-1 ADD CAP. VALUES	9/15/64	[illegible]	[illegible]	[illegible]

ITEM	SYMBOL	CA-3-10	DESCRIPTION	QTY
	CR1329		DIODE CLEVITE CGD 1032	
	R1330		CARBON FILM 700 Ω	
	CR1331		CGD 1032	
	CR1332		DIODE TRANSITRON IN191	
	CR1333		DIODE, CLEVITE CGD 1032	
	CR1334			
	C1335		DIODE TRANSITRON IN191	
	CR1336		DIODE CLEVITE CGD 1032	
	CR1337			
	CR1338			
	CR1339			
	CR1320			
	CR1321			
	CR1322			
	CR1323			
	CR1324			
	CR1325			
	CR1326			
	CR1327			
	CR1328			
	CR1329			
	CR1330			
	CR1331			
	CR1332			
	CR1333			
	CR1334			
	CR1335			
	CR1336			
	CR1337			
	CR1338			
	CR1339			
	CR1340			
	CR1341			
	CR1342			
	CR1343		DIODE TRANSITRON IN191	
	CR1344		DIODE CLEVITE CGD1032	
	CR1345			
	CR1346		DIODE TRANSITRON IN191	
	CR1347		DIODE CLEVITE CGD1032	

REF	DESCRIPTION	QTY



STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN

ADD TRANSPARENT SLEEVING TO COMPONENTS HAVING COPPER UNDERNEATH ON COMPONENT SIDE

TA-011773 REV H

ITEM	SYMBOL	DWG NO	DESCRIPTION	QTY /ASSY
		CE-012371-A	BOARD ASSY, CODE CONVERTER, RZ (LOWER)	
	R1330		RES FILM CB 1/4 W 10% 330Ω	1
	R1331		1Ω	1
	R1332		5.6K	1
	R1333		5.6K	1
	R1334		5.6K	1
	R1335		5.6K	1
	R1336		68Ω	1
	R1337		47K	1
	R1338		1.0K	1
	R1339		120K	1
	R1340		120K	1
	R1341		47K	1
	R1342		510K	1
	R1343		1.0K	1
	C1301	CAP ERIE	RPE3027H-150K10%, 15pf	1
	C1302		RPE3-006-X7D-470K	1
	C1303			1
	C1304		#831-000-U2J0-680K 10% 68pf	1
	C1305		150K 10% 15pf	1
	C1306		150K 10% 15pf	1
	C1307		680K 10% 68pf	1
	C1308		150K 10% 15pf	1
	C1309		680K 10% 68pf	1
	C1310		150K 10% 15pf	1
	C1311		#831-000-U2J0-330J 33pf	1
	C1312		831-127-15K10%15pf	1
	C1313		#831-000-U2J0-330J 33pf	1
	C1314		831-127-15K10%15pf	1
	C1315		[illegible]	1
	C1316		1.0pf	1
	C1317		1.0pf	1
	C1318		1.0pf	1
	C1319		1.0pf	1
	C1320		1.0pf	1
	CR1301		DIODE CLEVITE, CGD 1032	1
	CR1302			
	CR1303			
	CR1304		DIODE TRANSITRON IN191	1
	CR1305		DIODE CLEVITE CGD1032	1
	CR1306			
	CR1307			
	CR1308		DIODE TRANSITRON IN191	1
			JUMPER INSULATED	1
	R1301		RES FILM CB 1/4 W 10% 22Ω	1
	R1302		1.8K	1
	R1303		1.2K	1
	R1304		4.7K	1
	R1305		1.0K	1
	R1306		1.0K	1
	R1307		12K	1
	R1308		120K	1
	R1309		4.7K	1
	R1310		470Ω	1
	R1311		JUMPER	
	R1312		2.2K	1
	R1313		1.1K	1
	R1314		2.2K	1
	R1315		2.7K	1
	R1316		8.2K Ω	1
	R1317		9.1K	1
	R1318		1.0K	1
	R1319		120K	1
	P1320		1.2K	1
	R1321		6.1K	1
	R1322		820 Ω	1
	R1323		1.0K	1
	R1324		2.7K	1
	R1325		2.2K	1
	R1326		3.3K	1
	R1327		2.2K	1
	R1328		3.3K	1
	R1329		8.2K	1

NOTE:
1. INSTALL ITEM 2 UNDER Q1304 THRU 9 INCLUDING Q1310.
2. ALL ALLEN BRADLEY CB, YAW, 10% RESISTORS TO CONFORM TO MS35350

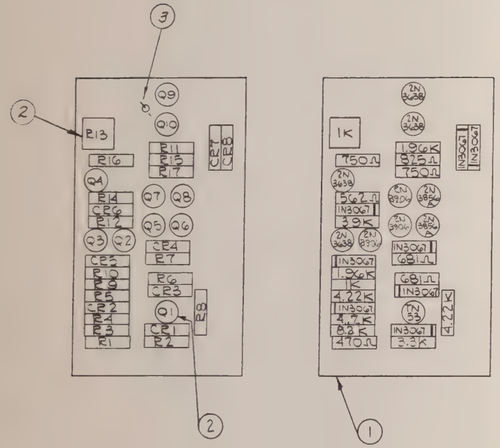
GPS- | CA-012472 | / | QTY /ASSY
FIRST PRODUCT | NEXT ASSEMBLY

DATA CONTROL SYSTEMS, INC.

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC ± 1/64 AND ± 0°30'
FLATNESS WITHIN ~ /IN
FRACTIONAL HOLES Ø ± 1/64
NOTE BREAK ALL SHARP CORNERS .005" .015"
SURFACE ROUGHNESS NOT TO EXCEED ✓

	DATE
DWN	[illegible]
CHKD	9/11/64
ENG	[illegible]
APP	9/11/64
SCALE	3/1

DO NOT SCALE DRAWING
MAT'L
FINISH
TA-011773 REV H
SHEET



	R1		RES, AB, EB, 1/2W, 10%	470Ω	1
	R2			3.3K	1
	R3		CB, 1/4 W, 10%	8.2K	1
	R4		CB, 1/4W, 10%	4.7K	1
	R5		ELECTRA,	4.22K	1
	R6			681Ω	1
	R7			681Ω	1
	R8		MFSC-D, 1/4W, 1%	4.22K	1
	R9		AB, CB, 1/4W 10%	1K	1
	R10		ELECTRA, MFSC-D 1/4W 1%	1.96K	1
	R11			1.96K	1
	R12		AB, CB, 1/4W, 10%	3.9K	1
	R13		POT, IRC 210-10	1K	1
	R14		ELECTRA	562Ω	1
	R15			825Ω	1
	R16		MFSC-D, 1/4W, 1%	750Ω	1
	R17			750Ω	1
	CR1		DIODE, CD	IN3067	1
	CR2				1
	CR3				1
	CR4				1
	CR5				1
	CR6				1
	CR7				1
	CR8			IN3067	1
	Q1		TRANS, SPRAGUE,	TN53	1
	Q2	NO SECOND CHOIC	MOTOROLA	2N3706	1
	Q3		FAIRCHILD,	2N3638	1
	Q4			2N3638	1
	Q5	NO SECOND CHOICE	MOTOROLA	2N3706	
	Q6		GE,	2N3856A	1
	Q7	NO SECOND CHOIC	MOTOROLA	2N3906	1
	Q8		GE,	2N3856A	1
	Q9		FAIRCHILD,	2N3638	1

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY REQ'D

1200 SERIES

	Q10		TRANS, FAIRCHILD, 2N3638	1
1		BD-015710	UPPER BD	1
2			TRANS PAD 10068	1
3			Z WIRE # AWG BUSS	1

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY REQ'D

REVISIONS						
SYM	DESCRIPTION	DATE	BY	CHK'D	APP'D
B	CA-3750 CHG'D RES. VALUES	6/1/67			
C	CA-4354 CHG'D TRANS. TYPES & VALUES	2/19/68			

DATA CONTROL SYSTEMS, INC.

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE BREAK ALL SHARP CORNERS .005"-.015"

TITLE: BD ASSY, GPD-6 BIT DETECTOR, UPPER BD

DO NOT SCALE DRAWING

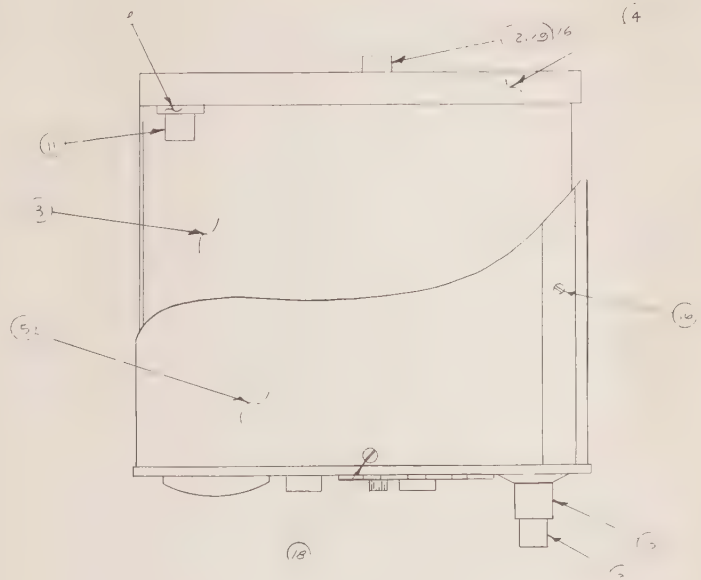
DWN 98 DATE 3/13/67
CHK'D
PROJ ENG 3/14/67
CH ENG
SCALE

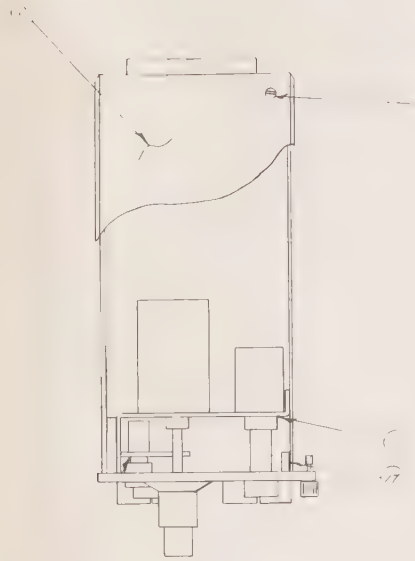
MAT'L
FINISH

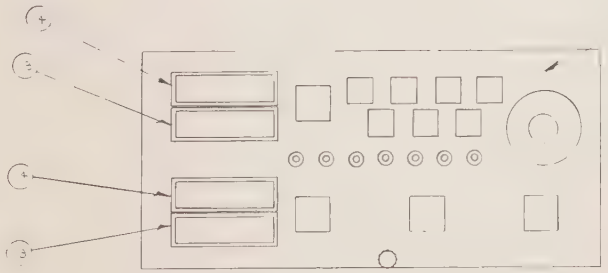
TA-015708

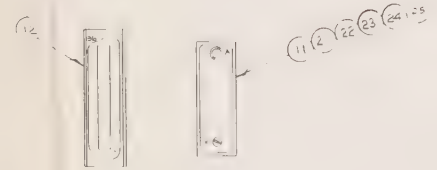
REV C

REVISIONS					
SYM	ZONE	DESCRIPTION	DATE	BY	CHK'D	APP'D
C		NOTE 1) CHG ITEM 9				
		2) ADDED ITEMS 17-20				
B		CA-3659 CHG'D ITEM 10 KNOB				
A		CA-3678 ADDED ITEMS 21 THRU 24	4/5/67			









VIEW FROM REAR
SHOWING ORIENTATION
OF CONNECTORS

NOTE 3 ITEMS 21, 22, 23 AND 24 ARE USED TO [illegible] RG 196/U CABLE [illegible] IS USED FOR #24 WIRE.

NOTES:
1) * = LATEST REVISION
2) ** = SCREW LENGTHS TO BE DETERMINED IN ACCORDANCE WITH DCS WORKMANSHIP MANUAL #AS-832011

ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
24		SEE NOTE 3	[illegible]	
23		SEE NOTE 3	RFD-26-1	
22		SEE NOTE 3	[illegible]	
21		MS-826003-*-01	INSERT, KNOB	
20		MS-826020-*-26	[illegible]	
19		MS-826006-*-40	SCR 4-40 [illegible]	
18		ED-015256	SHIM FROM [illegible]	
17		[illegible]	[illegible]	AR
16		MS-826020-*-26	[illegible]	AR
15		[illegible]	METER, FREQ SET	1
14		[illegible]	METER, PHASE ERROR	1
13		[illegible]	CONN, AMPHENOL [illegible]	1
12		[illegible]	CONN [illegible]	1
11		SL-[illegible]7760	KNOB, MODIFIED	1
10		MS-8[illegible]	[illegible]	1
9		[illegible]	FINAL SET ASSY - SHTS	1
8		CA-015288	BRACKET A	1
7		BF-015177	BRACKET	1
6		CF-015029	COVER, FAB	1
5		BF-015178	FAB, REAR [illegible]	1
4		CF-015015	[illegible]	1
3		CD-015032	[illegible]	1
2		CA-015293	[illegible]	1
1		[illegible]	[illegible]	1

REF	DESCRIPTION	QTY
	[illegible]	

TOLERANCES UNLESS OTHERWISE SPECIFIED		DATE
DECIMAL 3 PLACE ±	DRN RE	9/1/66
DECIMAL 2 PLACE ±	CHKD [illegible]	1-3-67
FRACTIONAL ± AND ± 0°30'	PROJ	
FLATNESS W THIN .005 IN	2ND	
FRACTIONAL HOLES	APP'D	
NOTE BREAK ALL SHARP CORNERS .005" DIA BURR & ROUGHNESS NOT TO EXCEED 125	APP'D	
MAT'L		
FIN SH		

NEXT ASSY	QTY
[illegible]	1

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

TITLE: FINAL ASSY GP-6
[illegible]

CODE IDENT NO	SIZE	REV
08539	DA-015186	D

SCALE [illegible] DO NOT SCALE D'WG DIMENSIONS IN INCHES SHEET OF

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
C	R+E Change - Changed PWR. Switch	1/26/67	H.W.M.	H.W.M.	
D	Added Notes on P & U Connections	2/20/67	H.W.M.	H.W.M.	

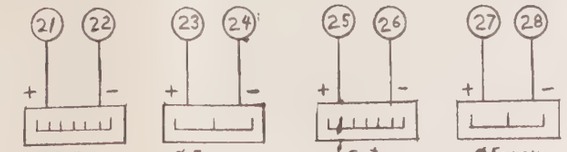
B	REV.

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY./ASSY

○ = Amphenol Connector J808

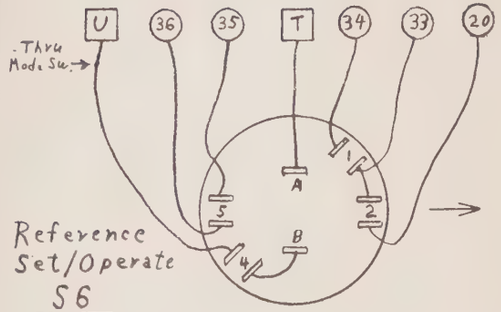
□ = Burndy Connector P807

Wiring of Mode and Format Switches Covered by BW-015297*-01

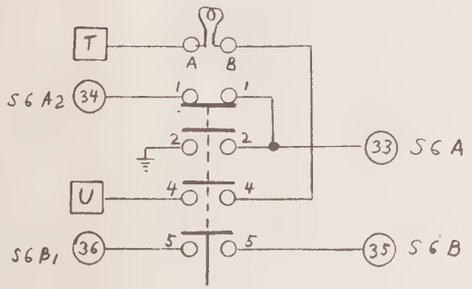


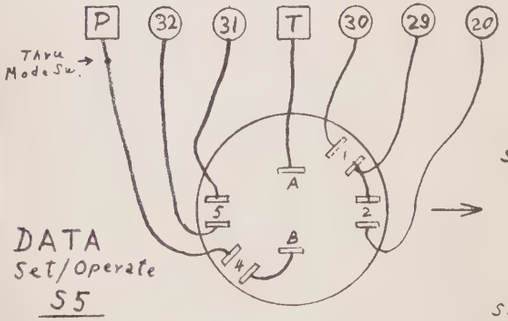
Data Reference

Meter Connections

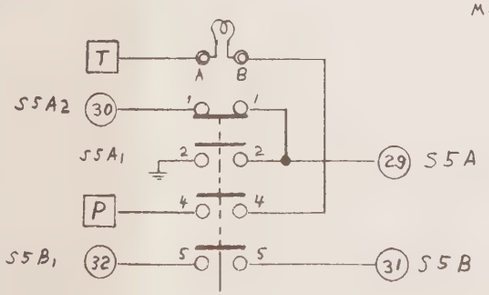


Reference Set/Operate S6





DATA Set/Operate S5

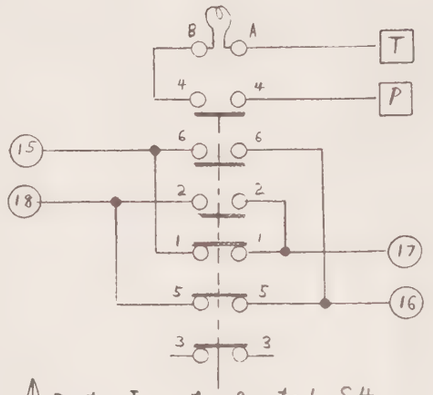


S5 and S6 Shown in Operate Position

Pender 1034L56W1/A

1NC-3NO

Momentary



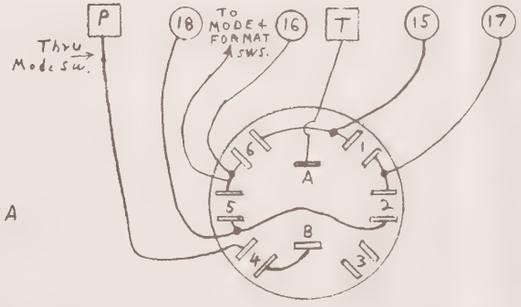
Data Invert Switch S4

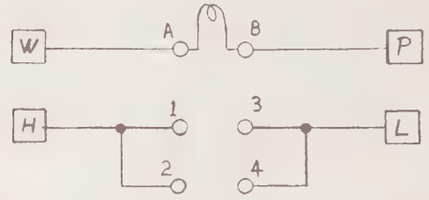
Shown in Normal Position

Pender 1122L56W1

3NC-3NO

Push-Push





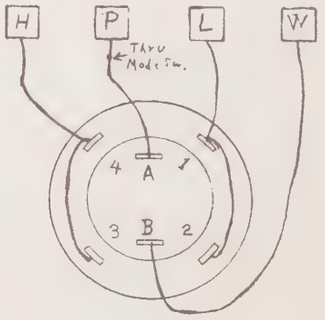
Power Switch S1

Shown in On position

Pender 1182L56G

DP-DT

Push-Push



REF.	DESCRIPTION	QTY

GPD-6

PRODUCT	NEXT ASSEMBLY	QTY./ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE SCHEMATIC ~ CONTROL UNIT
Ref. + Data Set/Operate, and Power Switches

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ✓

		DATE
DWN. H W M		12/13/66
CHKD. H W M		12/13/66
ENG. H W M		12/13/66
APP. B T		1/12/67
SCALE		

DO NOT SCALE DRAWING

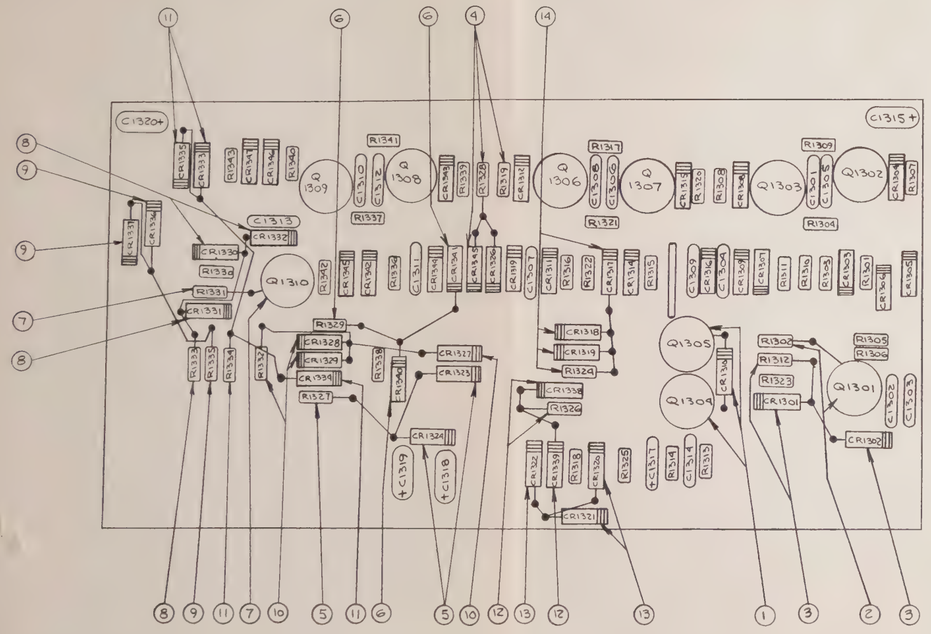
MAT'L

FINISH

BW-015297-*-02 REV. D

SHEET

REV	DESCRIPTION	DATE	DWN.	CHK	APP.



REF.	DESCRIPTION	QTY

GATES	COMPONENTS
3	CR1301
	CR1302
	R1312
4	CR1325
	CR1326
	R1328
5	CR1323
	CR1329
	R1327
6	CR1340
	CR1341
8	CR1330
	CR1331
	CR1332
	R1333
9	CR1336
	CR1337
	R1335
10	CR1327
	CR1328
	CR1329
	R1332
11	CR1333
	CR1334
	CR1335
	R1339
12	CR1338
	CR1339
	R1326
13	CR1320
	CR1321
	CR 1322
	R 1325
14	CR1317
	CR1318
	CR1319
	R1324

E.F.'S	COMPONENTS
INV SW 1	CR1310
	Q1304
	Q1305
2	Q1301
	R1302
7	Q1316
	R1331

	CR1312	DIODE, TRANSITRON, IN191	1
	CR1313	DIODE, CLEVITE, CGD1032	1
	CR1314		1
	CR1315	DIODE, TRANSITRON, IN191	1
	CR1316	DIODE, CLEVITE, CGD1032	1
	CR1317		1
	CR1318		1
	CR1319		1
	CR1320		1
	CR1321		1
	CR1322		1
	CR1323		1
	CR1324		1
	CR1325		1
	CR1326		1
	CR1327		1
	CR1328		1
	CR1329		1
	CR1330		1
	CR1331		1
	CR1332		1
	CR1333		1
	CR1334		1
	CR1335		1
	CR1336		1
	CR1337		1
	CR1338		1
	CR1339		1
	CR1340		1
	CR1341		1
	CR1342		1
	CR1343	DIODE, TRANSITRON, IN191	1
	CR1344	DIODE, CLEVITE, CGD1032	1
	CR1345		1
	CR1346	DIODE, TRANSITRON, IN191	1
	CR1347	DIODE, CLEVITE, CGD1032	1

NOTES:
1) REF TA-011773
2) INDICATED CONNECTIONS ARE ELECTRICAL, PHYSICAL CONNECTIONS MAY BE ON EITHER OR BOTH SIDES OF BOARD.
3) REF SCHEMATIC GW-012731

TY-013026 A

	R1333	RES, AB, CB, 1/4W, 10%, 5.6K	1
	R1334	5.6K	1
	R1335	5.6K	1
	R1336	820Ω	1
	R1337	4.7K	1
	R1338	1.0K	1
	R1339	120K	1
	R1340	120K	1
	R1341	4.7K	1
	R1342	560Ω	1
	R1343	1.0K	1
	C1301	CAP, CERAMIC DISC, 150K, 10%, 15μμf	1
	C1302	680K, 10%, 68μμf	1
	C1303	680K, 10%, 68μμf	1
	C1304	680K, 10%, 68μμf	1
	C1305	150K, 10%, 15μμf	1
	C1306	150K, 10%, 15μμf	1
	C1307	680K, 10%, 68μμf	1
	C1308	150K, 10%, 15μμf	1
	C1309	680K, 10%, 68μμf	1
	C1310	150K, 10%, 15μμf	1
	C1311	680K, 10%, 68μμf	1
	C1312	150K, 10%, 15μμf	1
	C1313	680K, 10%, 68μμf	1
	C1314	150K, 10%, 15μμf	1
	C1315	CAP, KEMET, KIP35, 35V, 20%, 10μf	1
	C1316	10μf	1
	C1317	1.0μf	1
	C1318	1.0μf	1
	C1319	1.0μf	1
	C1320	1.0μf	1
2		JUMPER, INSULATED	1
	CR1301	DIODE, CLEVITE, CGD1032	1
	CR1302		1
	CR1303		1
	CR1304	DIODE, TRANSITRON, IN191	1
	CR1305	DIODE, CLEVITE, CGD1032	1
	CR1306		1
	CR1307		1
	CR1308	DIODE, TRANSITRON, IN191	1
	CR1309	DIODE, CLEVITE, CGD1032	1
	CR1310	CTP700A	1
	CR1311	CGD1032	1

ITEM	BY/SYMBOL	DWG. NO.	DESCRIPTION	QTY
1		MILTON ROY A10042	PAD, TRANS, 8095	10
	Q1301		TRANS, T.I., GM-592-A	1
	Q1302			1
	Q1303			1
	Q1304			1
	Q1305			1
	Q1306			1
	Q1307			1
	Q1308			1
	Q1309			1
	Q1310			1
	R1301		RES, AB, CB, 1/4W, 10%, 220Ω	1
	R 302		1.8K	1
	R1303		1.2K	1
	R1304		4.7K	1
	R1305		1.0K	1
	R1306		1.0K	1
	R1307		120K	1
	R1308		120K	1
	R1309		4.7K	1
	R1310		1.2K	1
	R1311		1.0K	1
	R1312		2.7K	1
	R1313		2.7K	1
	R1314		22K	1
	R1315		2.7K	1
	R1316		820Ω	1
	R1317		4.7K	1
	R1318		1.0K	1
	R1319		120K	1
	R1320		120K	1
	R1321		4.7K	1
	R1322		820Ω	1
	R 323		1.0K	1
	R 324		2.7K	1
	R1325		2.7K	1
	R1326		3.3K	1
	R1327		5.6K	1
	R1328		3.3K	1
	R1329		8.2K	1
	R1330		220Ω	1
	R1331		1.8K	1
	R1332		5.6K	1

GPS-5		
FIRST PRODUCT	NEXT ASSEMBLY	QTY. SEE↑

DATA CONTROL SYSTEMS, INC.

TITLE: GATE LOCATION, CODE CONVERTER, RZ (LOWER)

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC ± 1/64 ANG ± 0°30'
FLATNESS WITHIN ~ IN.
FRACTIONAL HOLES .0 + 1/64
NOTE: BREAK ALL SHARP CORNERS .008"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

DO NOT SCALE DRAWING

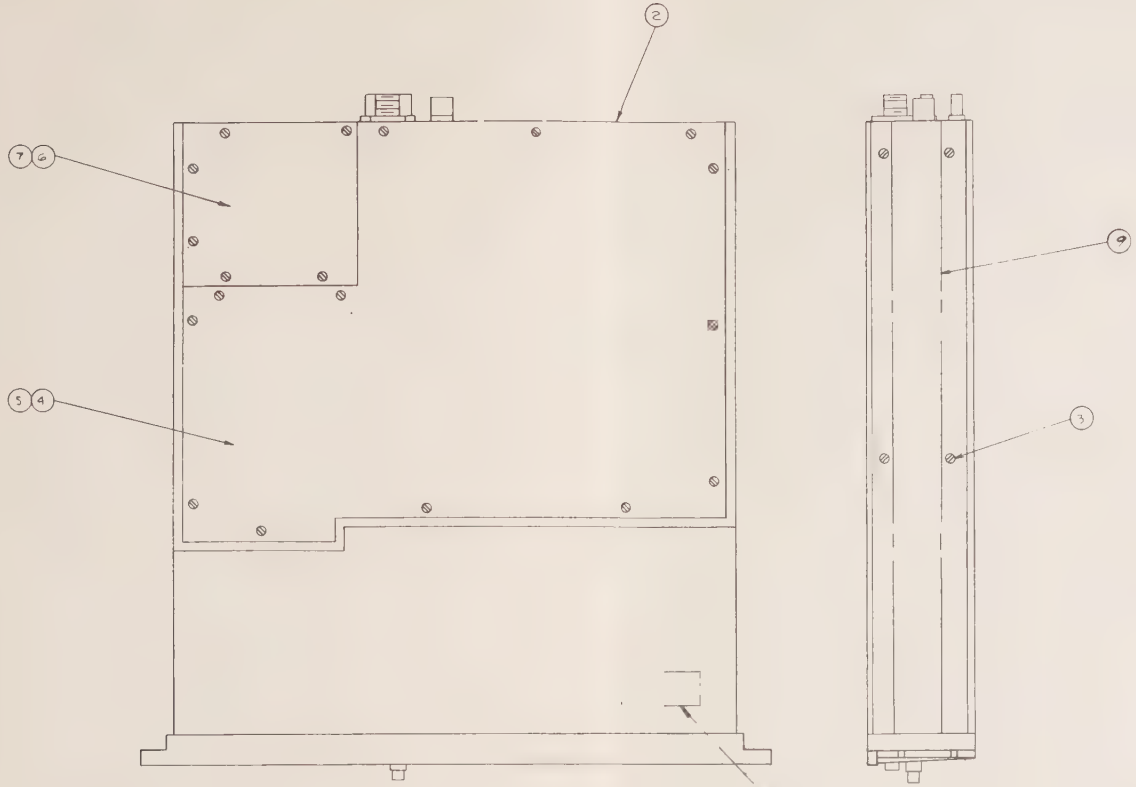
DWN	DH	12/16/69
CHKD		1/16/70
ENG.		1/16/70
APP.		1/16/70
SCALE	2X	

MAT'L ~
FINISH ~

TY-013026 REV A

SHEET

REVISIONS						
SYM	ZONE	DESCRIPTION	DATE	BY	CHK'D	APP'D



STAMP MODEL NO., SERIAL NO. & FINAL ASSY NO. AS REQD. IN 1/8 HIGH CONTRASTING CHARACTERS

NOTE.
1. * ORTIONAL SLIDE SUPPLIED ON REQUEST ONLY

ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
* 9			SLIDE GRANT "7725"	2
8		CA-015186	CONTROL UNIT ASSY	1
7			SCREW "4-40 NC-2A-3/16 BHMS, SCP	6
6		BD-011420	COVER, FAN	1
5			SCREW "4-40 NC-2A-3/16 BHMS, S.C.P.	12
4		CI-015274	COVER, CHASSIS	1
3			SCREW "6-32 NC-2A-7/16, 100° FHMS, SCP	8
2		DA-015273	CHASSIS ASSY, POWER SUPPLY	1
1		CA-011501	MODULAR HOUSING ASSY	1

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PLACE ± .005
DECIMAL 3 PLACE ± .010
FRAC. ± 1/64 AND ± 0° 30'
FLATNESS WITHIN .005 IN
FRACTIONAL HOLES ± 1/64
NOTE BREAK ALL SHARP CORNERS .005" MAX
SURFACE ROUGHNESS NOT TO EXCEED 125
MAT'L
FINISH

	DATE
DWN	11/6/67
CHK'D	11/9/67
PROJ. ENG	11/11/67
APP'D	11/12/67
APP'D	

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

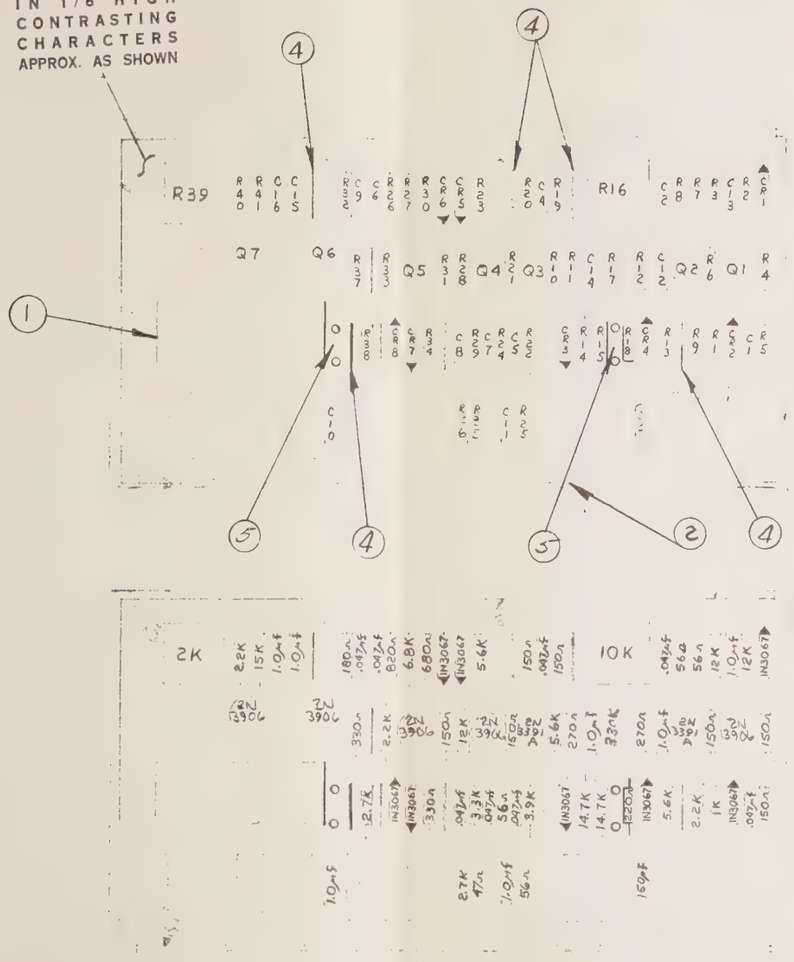
TITLE: FINAL ASSY GPD-6

CODE IDENT NO. | SIZE: D | DA-015271 | REV: A

SCALE | SHEET

GPD-6 | NEXT ASSEMBLY
PRODUCT

STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN



DC RESTORER + LIM.

1000 SERIES

DC. RESTORER & LIMITER BD

GPS-5 AND 6
GPD-6

	ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY REQ'D
		R1	1K	AB,CB, 10%, 1/4W	
		R2	12K		
		R3	12K		
		R4	150Ω		
		R5	150Ω		
		R6	150Ω		
		R7	56Ω		
		R8	56Ω		
		R9	2.2K	AB, EB, 10% 1/2W	
		R10	5.6K	AB, CB, 10%, 1/4W	
		R11	270Ω		
		R12	270Ω		
		R13	5.6K		
		R14	14.7K	ELECTRA MFSC-D 1%, 1/4W	
		R15	14.7K	ELECTRA MFSC-D 1%, 1/4W	
		R16	10K	IRC CIRCUITRIM 201-10-10K	
		R17	330K	AB,CB 10%, 1/4W	
		R18	220Ω		
		R19	150Ω		
		R20	150Ω		
		R21	150Ω		
		R22	3.9K		
		R23	5.6K		
		R24	56Ω		
		R25	56Ω		
		R26	820Ω		
		R27	6.8K		
		R28	12K		
		R29	3.3K		
		R30	680Ω		
		R31	150Ω		
		R32	180Ω		
		R33	2.2K		
		R34	330Ω		
		R35	47Ω		
		R36	2.7K		

1000 SERIES

DC RESTORER & LIMITER GPS-5 AND 6 / GPD-6

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY. REQ'D
	R37	330 Ω	AB, CB 10%, ¼W	
	R38	2.7K	AB, CB 10%, ¼W	
	R39	2K	IRC CIRCUITRIM 201-10-2K	
	R40	9.2K	AB, CB 10%, ¼W	
	R41	15K	AB, CB 10%, ¼W	
	C1	.047MF	SPRAGUE, 3C15 25V 20%	
	C2	.047MF	SPRAGUE 3C15 25V 20%	
	C3	150 PF	ERIE, 831-000-X5F0-151K, 10%	
	C4	.047MF	SPRAGUE, 3C15 25V 20%	
	C5	.047MF	〃	
	C6	.047MF	〃	
	C7	.047MF	〃	
	C8	.047MF	〃	
	C9	.047MF	〃	
	C10	1.0MF	5C13 25V 20%	
	C11	1.0MF	〃	
	C12	1.0MF	〃	
	C13	1.0MF	〃	
	C14	1.0MF	〃	
	C15	1.0MF	〃	
	C16	1.0MF	〃	
	CR1	IN3067		
	CR2	IN3067		
	CR3	IN3067		
	CR4	IN3067		
	CR5	IN3067		
	CR6	IN3067		
	CR7	IN3067		
	CR8	IN3067		

DC RESTORER & LIMITER. GPS-5 AND 6 / GPD-6

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY. REQ'D
	Q1	2N3906	NO SECOND CHOICE MANUFACTURER	
	Q2	2N3391A		
	Q3	2N3391A		
	Q4	2N3906	MANUFACTURER - NO SECOND CHOICE	
	Q5			
	Q6			
	Q7			
1		TA-015723	PLUG-IN. ASSY	1
2		CF-011290	BD. FAB, REST. + LIM.	1
4			JUMPER #24 WIRE BLK INSULATED	A/R
5			JUMPER, GPS-5 & GPS-6 ONLY	

		DATE		CHK'D	APP'D
B	REF 1) ADDED ITEMS 4 & 5 2) CHANGED ITEM 1	12/22/66	RTW		
C	(R46) 2N4250 WAS 2N3906	3/3/67	RTW		
D	CA-3850 CHG'D CAP. STYLE	7/11/67			
E	CA-3910 CHG'D HARDWARE ADDED NOTES 1 + 2	9/8/67			
F	CA-4354 CHG'D TRANS TYPES & VALUE	3-29-68		GR	GR

NOTES:
* 1) -1 DESIGNATES THE USE OF ITEM #5.
* 2) -2 DESIGNATES THE OMISSION OF ITEM #5.

DATA CONTROL SYSTEMS, INC.

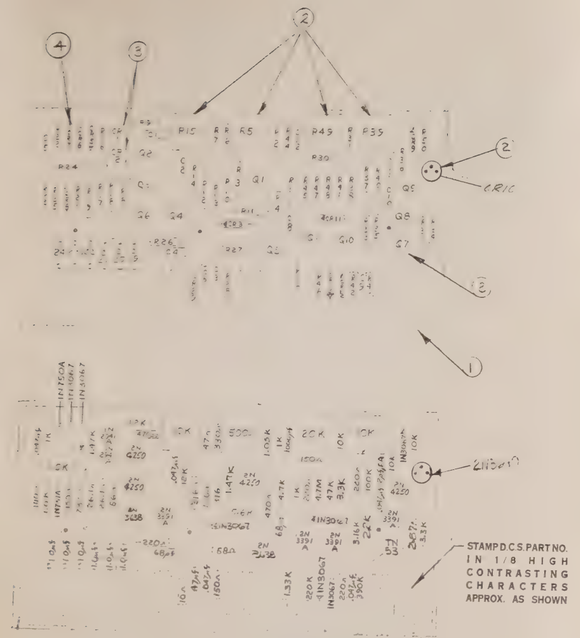
TITLE: RESTORER BD. ASSY, GPD-6

DWN WB 7/1/66 | CHKD RTW 8/26/66 | PROJ ENG. H.W.M 8/26/66 | M. ENG PA+ 8/26/66 | SCALE

DO NOT SCALE DRAWING

MATL | FINISH

GA-015166 | DASH NO. * | REV. F



VCO BD

1100 SERIES

ITEM	SYMBOL	PART NO.	DESCRIPTION	QTY REQ'D
	R1	4.7K	AB, CB 10% ¼W	
	R2	1.05K	ELECTRA MFG-D 1% ¼W	
	R3	1.47K	ELECTRA MFG-D 1% ¼W	
	R4	470Ω	AB, CB 10% ¼W	
	R5	50Ω	TRW CIRCUITRIM 201-10-50Ω	
	R6	330Ω	ELECTRA MFG-D 1% ¼W	
	R7	47Ω		
	R8	56Ω		
	R9	1.2K		
	R10	316Ω	ELECTRA MFG-D 1% ¼W	
	R11	5.6K	AB, CB 10% ¼W	
	R12	316Ω	ELECTRA MFG-D 1% ¼W	
	R13	100Ω	AB, CB 10% ¼W	
	R17	12K		
	R15	10K	TRW CIRCUITRIM 201-10-10K	
	R16	1.47K	ELECTRA MFG-D 1% ¼W	
	R17	26.1Ω		
	R18	26.1Ω		
	R19	1/32Ω		
	R20	1.33K		
	R21	150Ω	AB, CB 10% ¼W	
	R22	1K		
	R23	100Ω		
	R24	1.0K	ELECTRA MFG-D 1% ¼W	
	R25	1.0K		
	R26	220Ω	AB, CB 10% ¼W	
	R27	68Ω		
	R28	150Ω		
	R29	12Ω		
	R30	150Ω		
	R31	12K		
	R32	2.87K	ELECTRA MFG-D 1% ¼W	
	R33	3.16K		
	R34	2.2K	AB, CB 10%	
	R35	2.2K	AB, EB 10% ½W	
	R36	10K	AB, CB 10% ¼W	

1100 SERIES

	CR1	IN231 E	FIRST V.E.	
	CR2	IN231 E		
	CR3	IN3067		
	CR4	IN3067		
	CR5	IN3067		
	CR6	IN750A	CONT. DIVICES	
	CR7	IN751A		
	CR8	IN3067		
	CR9	2N3640	TRANSIST CONNECTED AS A DIODE	
	CR10	IN3067		
	CR11	IN3067		
	CR12	IN3067		
	Q1	2N4250		
	Q2	2N4250		
	Q3	2N4250		
	Q4	2N3250 E		
	Q5	2N3638	FAIRCHILD NO SECOND CHOICE	
	Q6	2N3638	FAIRCHILD	
	Q7	JN53	SPRAGUE, 2ND CHOICE 2N2218	
	Q8	2N3250 A		
	Q9	2N4250		
	Q10	2N3250 A		
	Q11	2N3250 A		
1		CF-012336	BD FAB, VCO	1
2			TRANS PADS, ROSS #A0006B	6
3			TRANS PADS, ROSS #A10042	2

ITEM	SYMBOL	PART NO.	DESCRIPTION			QTY REQ'D
	OUTSIDE DIA	INSIDE DIA.	LENGTH	MATERIAL	DWG NO.	
4	3.5MM	1.2 MM	5.2 MM	SIFERRIT 950 M25, 1500 N4	6ZUB SPK 93H103	

REVISIONS					
SYM	DESCRIPTION	DATE	BY	CHK'D	APP'D
C	ITEM 1 WAS CF-015196 (-A,-B,-E)	1/9/67	RTW		
	REF 2N4250 WAS 2N3906	4/16/67	RTW		
D	CA-3750 CHGD COMP. VALUES	6/15/67	RTW	6/27/67	JLG
E	CA-3850 CHG'D CAP. STYLE	7/11/67	RTW		
F	CA-3881 ADD C1107	9/6/67	RTW		
G	CHANGE SIZE	12/27/67	RTW		
H	CA-4005 CHG TRANS VALUE ADDED NOTE #1	2/6/68	RTW		
J	CA-4230 ADDED ITEM #4	2/6/68	RTW		
K	CA-4263 CHG R1138 FROM 6.8K TO 3.3K	2/14/68	RTW		

NOTES:
1) Q1105 TO USE 2N3638 ONLY; NO SECOND CHOICE

DATA CONTROL SYSTEMS, INC.

VCO BOARD ASSY GPD-6

UNLESS OTHERWISE SPECIFIED
DECIMAL 3 PLACE ± .005
DECIMAL 2 PLACE ± .010
FRAC ± 1/64 ANG ± 0°30'
FLATNESS WITHIN .001 IN
FRACTIONAL HOLES ± 1/64
NOTE BREAK ALL SHARP

DRWN WB 6/30/66
CHKD RTW 8/25/66
PROJ
ENG
CH
ENG PAT 7/24/69

MATL
FINISH

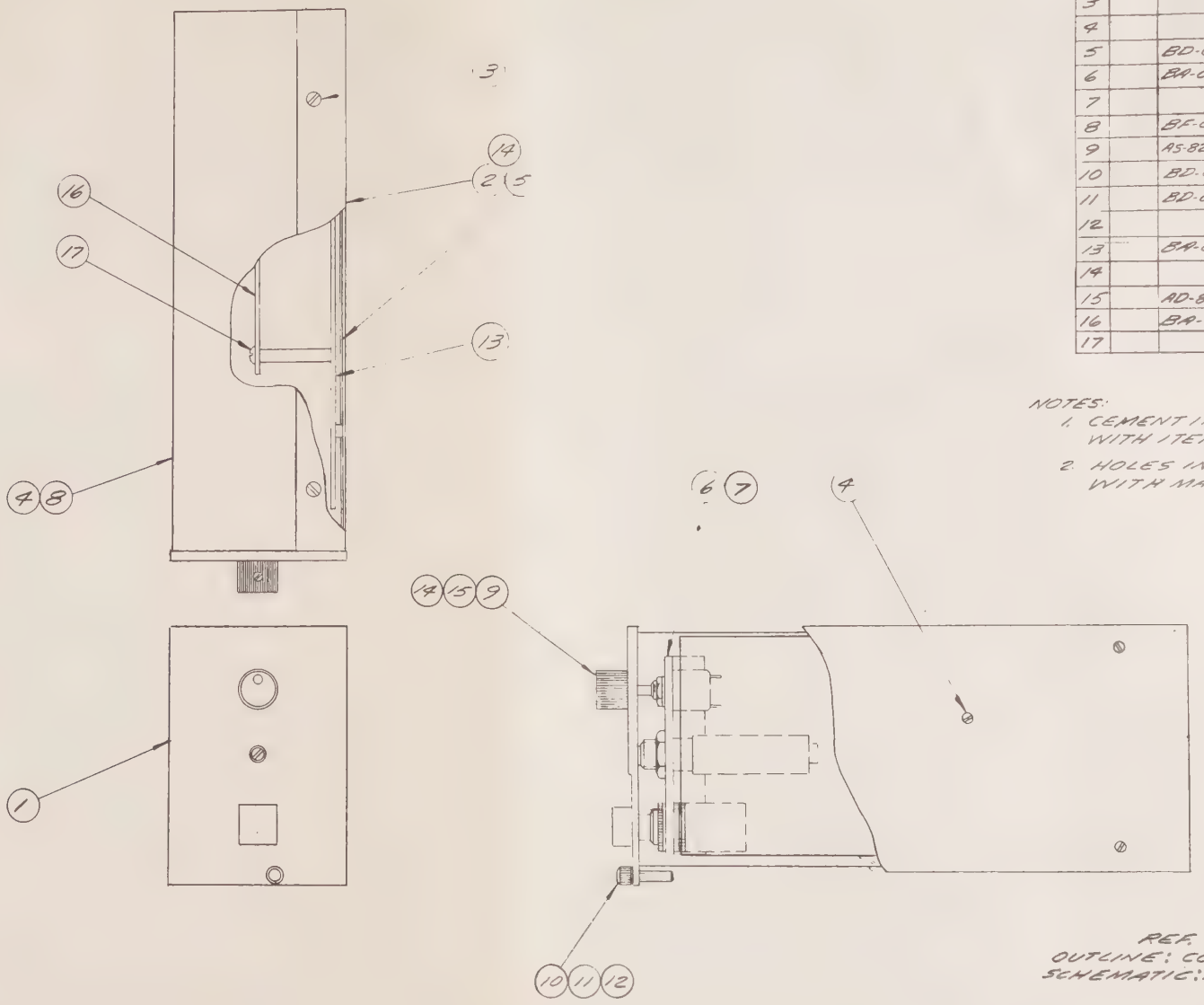
DO NOT SCALE DRAWING

6A-015154 REV K

REV	DATE	DESCRIPTION	BY	CHK'D	APP'D
E	11/18/64	CI-3167. CHG'D ITEM 2.	P.I.		

ITEM	SYMBOL	DWG NO.	DESCRIPTION	QTY. ASSY
1		BD-012773	FRONT PANEL	1
2		BD-011126	CHASSIS	1
3			SCREW, #4-40 NC-2A X 3/16 100° FHMS STCD. PL.	4
4			SCREW, #2-56 NC-2A X 3/16 100° FHMS ST CR PL.	11
5		BD-012783	INSULATOR, CHASSIS	1
6		BA-012784	BRACKET ASSY	1
7			SCREW, #4-40 NC-2A X 1/4 100° FHMS ST CD PL.	2
8		BF-012759	COVER FAB	1
9		AS-826004-B-01	KNOB	1
10		BD-008912	SCREW, CAPTIVATED	1
11		BD-008929	KNOB, CAPTIVATED	1
12			ROLL PIN ESNA RP-B79-012-062-0187	1
13		BA-012749	EL. ASSY, LOWER	1
14			ADHESIVE ARMSTRONG A-11	A/R
15		AD-826003-A03	INSERT	1
16		BA-012750	BD. ASSY, UPPER	1
17			SCREW #2-56 NC-2A X 1/4 LG FHMS S.C. PL.	4

NOTES:
1. CEMENT ITEM 5 TO ITEM 2 WITH ITEM 14
2. HOLES IN ITEM 5 TO CORRESPOND WITH MATING HOLES IN ITEM 2



REF. DRAWINGS
OUTLINE: CO-012796
SCHEMATIC: BW-012799

C.A. 012670 B

DWG.	DESCRIPTION	QTY.

GPS-5/TU		~
PRODUCT	NEXT ASSEMBLY	QTY. ASSY

DATA CONTROL SYSTEMS, INC.

TITLE: FINAL ASSY, DOUBLE MODULE TUNING UNIT

TOLERANCES- UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~/.001
FRACTIONAL HOLES -0, + 1/64
NOTE BREAK ALL SHARP CORNERS .005"-.010"

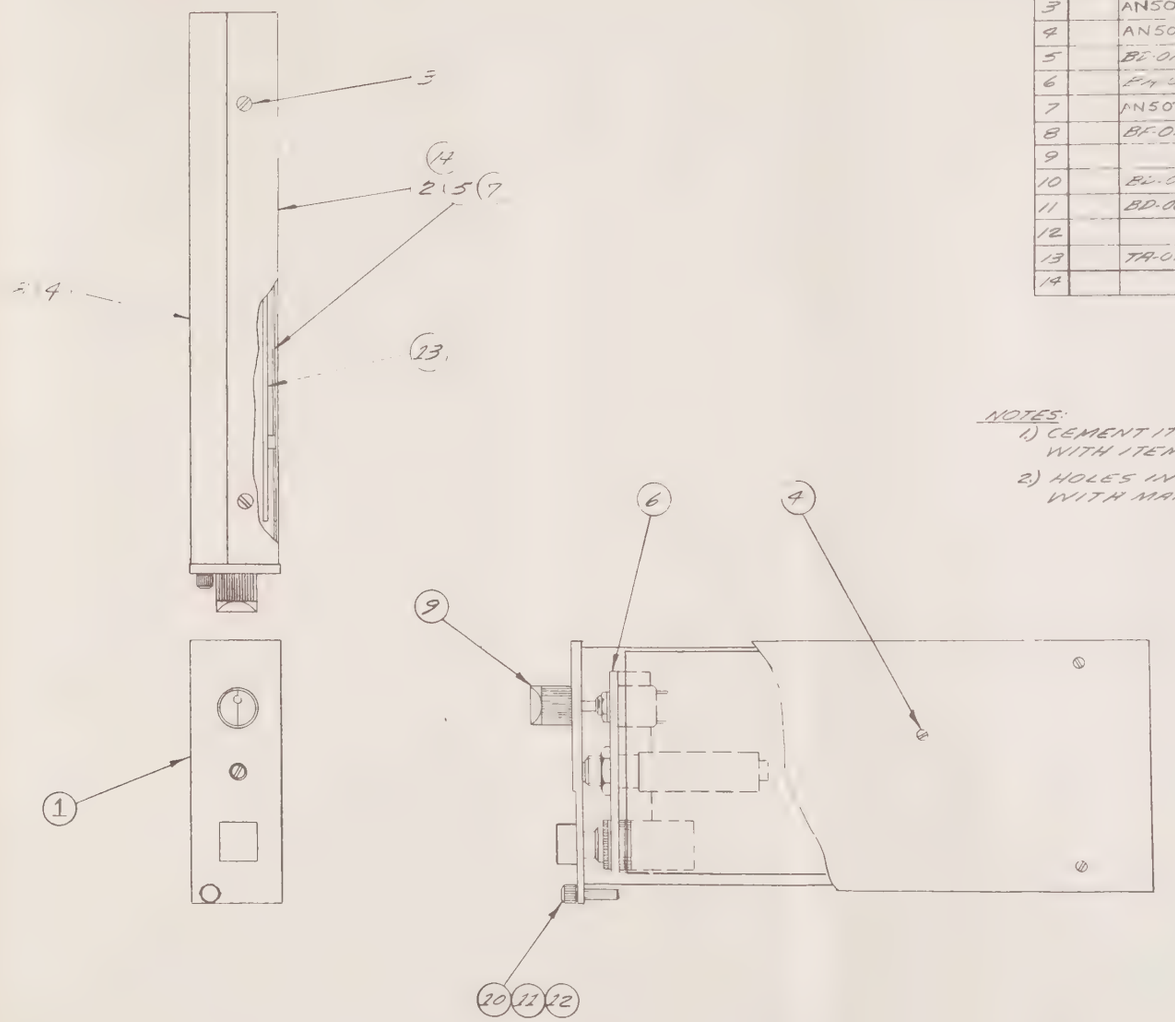
		DATE
DWN	PJH	9/30/64
CHKD	[illegible]	10/7/64
PROJ ENG	[illegible]	10/8/64
CH ENG	[illegible]	10/7/64
SCALE	FULL	

DO NOT SCALE DRAWING
MAT'L
FINISH

C.A. 012760 B

REV	DATE	DESCRIPTION	BY	CHK'D	ENG'G
B	9/1/63	CA-2768-CHG'D. ITEM 2 & 7	RJH	KDG	PMA

ITEM	SYMBOL	DWG NO	DESCRIPTION	QTY ASSY
1		BD-011125	FRONT PANEL	1
2		BD-011126	CHASSIS	1
3		AN507-440-3	SCREW #4-40 NC-2A X 3/16 100° FHMS STCD PL	4
4		AN507-256-3	SCREW #2-56 NC-2A X 3/16 100° FHMS ST CD PL	11
5		BD-011136	INSULATOR, CHASSIS	1
6		PA 0116-40	BRACKET ASSY	1
7		AN507-440-4	SCREW #4-40 NC-2A X 3/16 100° FHMS ST CD PL	2
8		BF-011128	COVER	1
9			KNOB RAYTHEON 50-1-HG W.I.	1
10		BD-008916	SCREW, CAPTIVATED	1
11		BD-008924	KNOB, CAPTIVATED	1
12			DOLL P-V ESNA RP-B7-012-062-0187	1
13		TA-011122	ASSY-TUNING UNIT BD.	1
14			ADHESIVE EASTMAN 910	A/R



NOTES:
1) CEMENT ITEM 5 TO ITEM 2 WITH ITEM 14
2) HOLES IN ITEM 5 TO CORRESPOND WITH MATING HOLES IN ITEM 2

CA-011178 REV B

REV	DESCRIPTION	QTY

GPS-5/TU — PRODUCT — NEXT ASSEMBLY — QTY/ASSY

DATA CONTROL SYSTEMS, INC.

TITLE: ASSY-TUNING UNIT

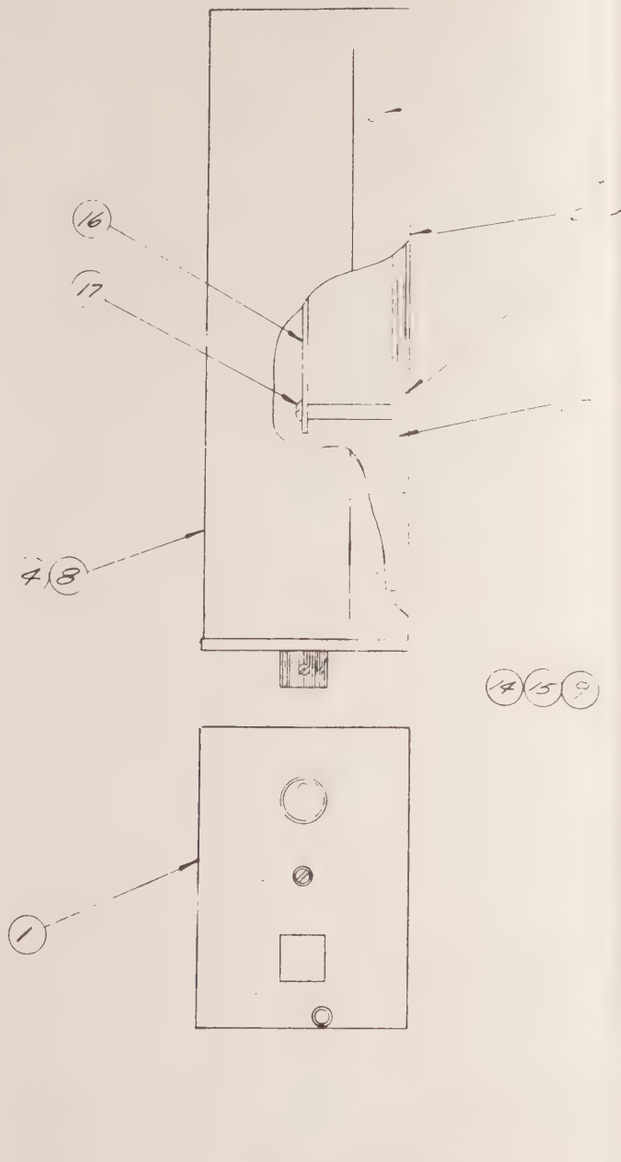
TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL 3 PLACE ± .005
DECIMAL 2 PLACE ± .010
FRAC ± 1/64 ANG ± 0°30'
FLATNESS WITHIN .../IN
FRACTIONAL HOLES Ø .4 1/64
NOTE BREAK ALL SHARP CORNERS .005" - .015"

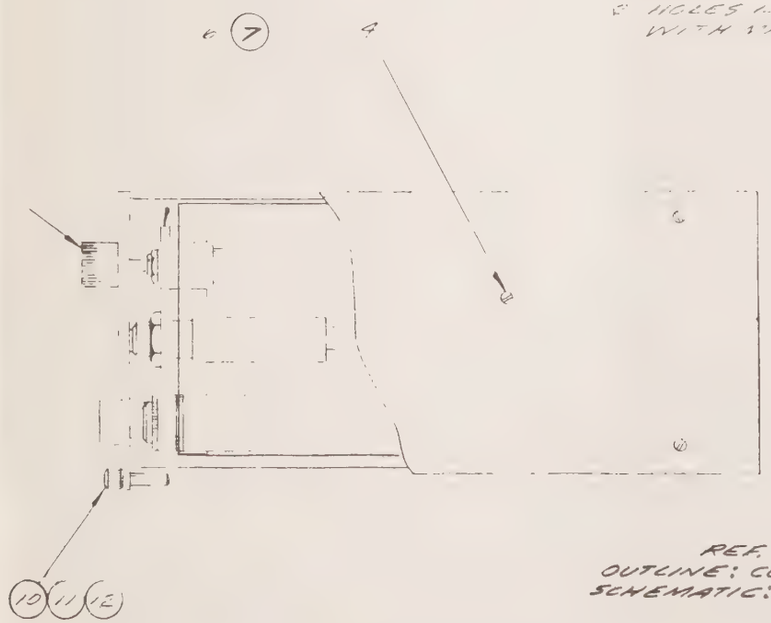
		DATE
DWN	RJH	8/29/63
CHKD	[illegible]	9-6-63
PROJ ENG	WJ	9/4/63
CH. ENG.	WJ	9/4/63
SCALE	FULL	

DO NOT SCALE DRAWING
MAT'L
FINISH

CA-011178 REV. B

NO.	DATE	DESCRIPTION	BY





ITEM	SYMBOL	DWG NO	DESCRIPTION	QTY PER
1		CD-015902	FRONT PANEL	1
2		BD-011126	CHASSIS	1
3			SCREW, #4-40 UNC-2A x 5/16 100° FLHMS STCSK	4
4			SCREW, #2-56 UNC-2A x 3/16 100° FLHMS ST CSK	11
5		BD-012793	INSULATOR, CHASSIS	1
6		BA-015901	BRACKET ASSY	1
7			SCREW, #4-40 UNC-2A x 1/4 100° FLHMS ST CSK	2
8		BF-012759	COVER FAB	1
9		AS-8260N-B-01	KNOB	1
10		P/N 008912	SCREW, CAPTIVATED	1
11		P/N 008924	KNOB, CAPTIVATED	1
12			BOLT, BDY ESNA P/N B7-012-062-0187	1
13		TA-015305	BD. ASSY, LOWER	1
14			SCOTCH-WELD ADHESIVE 2214 TWO PART EPOXY	A/R
15		AD-826003-A03	INSERT	1
16		TA-015306	BD. ASSY, UPPER	1
17			SCREW, #2-56 UNC-2A x 5/16 FLHMS S.C.A.	4

NOTES
1. CEMENT ITEM 4 TO ITEM 2 WITH ITEM 14
2. HOLES IN ITEM 5 TO CORRESPOND WITH MTG HOLES IN ITEM 2

REF. DRAWINGS
OUTLINE: CO-012796
SCHEMATIC: BW-012799

C.A. 012670

DESCRIPTION	QTY

6PD-6/F	
PRODUCT	NEXT ASSEMBLY

DATA CONTROL SYSTEMS, INC.

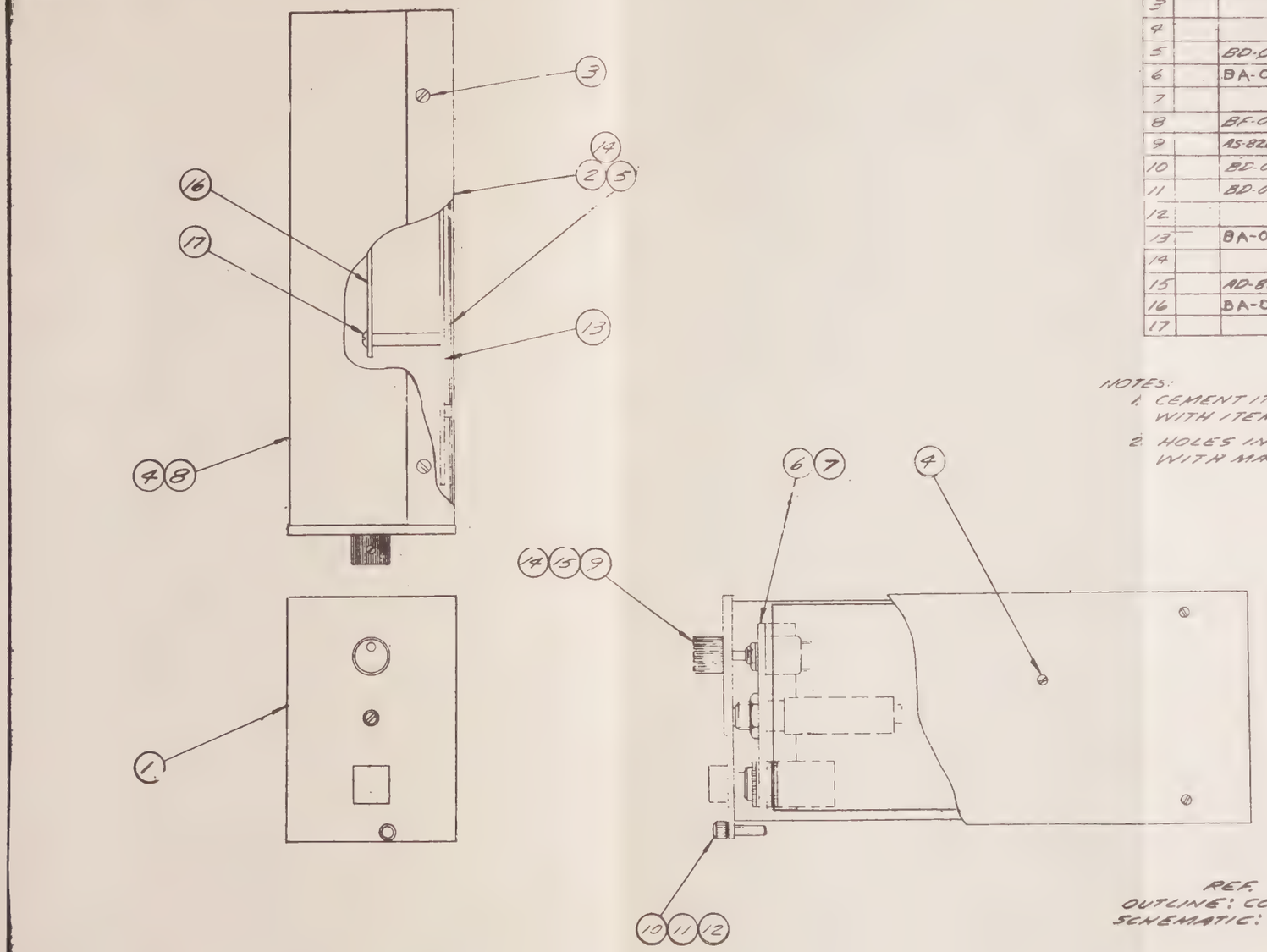
TITLE: FINAL ASSY, DOUBLE MODULE TUNING UNIT

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL 3 PLACE ± .005
DECIMAL 2 PLACE ± .010
FRAC ± 1/64 ANG ± 0°30'
FLATNESS WITHIN .001 IN.
FRACTIONAL HOLES ØA ± 1/64
NOTE BREAK ALL SHARP CORNERS .005/.015

		DATE
DWN	P.J.H.	9/20/65
CHKD	[illegible]	9-29-64
PRO		MAT'L
ENG	[illegible]	10/5/64
CH. ENG	[illegible]	10/7/64
SCALE	FULL	FINISH

DO NOT SCALE DRAWING

C.A.-015900 REV. A



ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY.
1		BD-015303	FRONT PANEL	1
2		BD-011126	CHASSIS	1
3			SCREW 4-40 UNC-2AX1/4 100° FHMS. SSCP.	4
4			SCREW 2-56UNC-2AX3/16 100° FHMS. ST. CAD.	AR
5		BD-012783	INSULATOR, CHASSIS	2
6		BA-015302	BRACKET ASSY.	4
7			SCREW 4-40 UNC-2AX1/4 100° FHMS ST. STD. BR.	2
8		BF-012759	COVER-FAB	1
9		AS-826001-B-01	KNOB	1
10		BD-008912	SCREW, CAPTIVATED	1
11		BD-008929	KNOB, CAPTIVATED	1
12			ROLL PIN ESNA AD-879-012-062-0187	1
13		BA-015305	BD. ASSY, LOWER	1
14			ADHESIVE ARMSTRONG A-11	AR
15		AD-826003-A13	INSERT	1
16		BA-015306	BD. ASSY, UPPER	1
17			SCREW 4-36 UNS-2A X 1/16 PHMS SS CA	4

NOTES:
1. CEMENT ITEM 5 TO ITEM 2 WITH ITEM 14
2. HOLES IN ITEM 5 TO CORRESPOND WITH MATING HOLES IN ITEM 2

REF. DRAWINGS
OUTLINE: CO-015308
SCHEMATIC: CW-015307

DATA CONTROL SYSTEMS, INC.

TITLE: FINAL ASSY, DOUBLE MODULE TUNING UNIT

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 AND ± 0°30'
FLATNESS WITHIN .001
FRACTIONAL HOLES .01 ± 1/64
NOTE: BREAK ALL SHARP CORNERS .005 MAX

DWN
CHKD
PROD.
ENG.
CH.
ENG.
SCALE

DO NOT SCALE DRAWING

MAT'L
FINISH

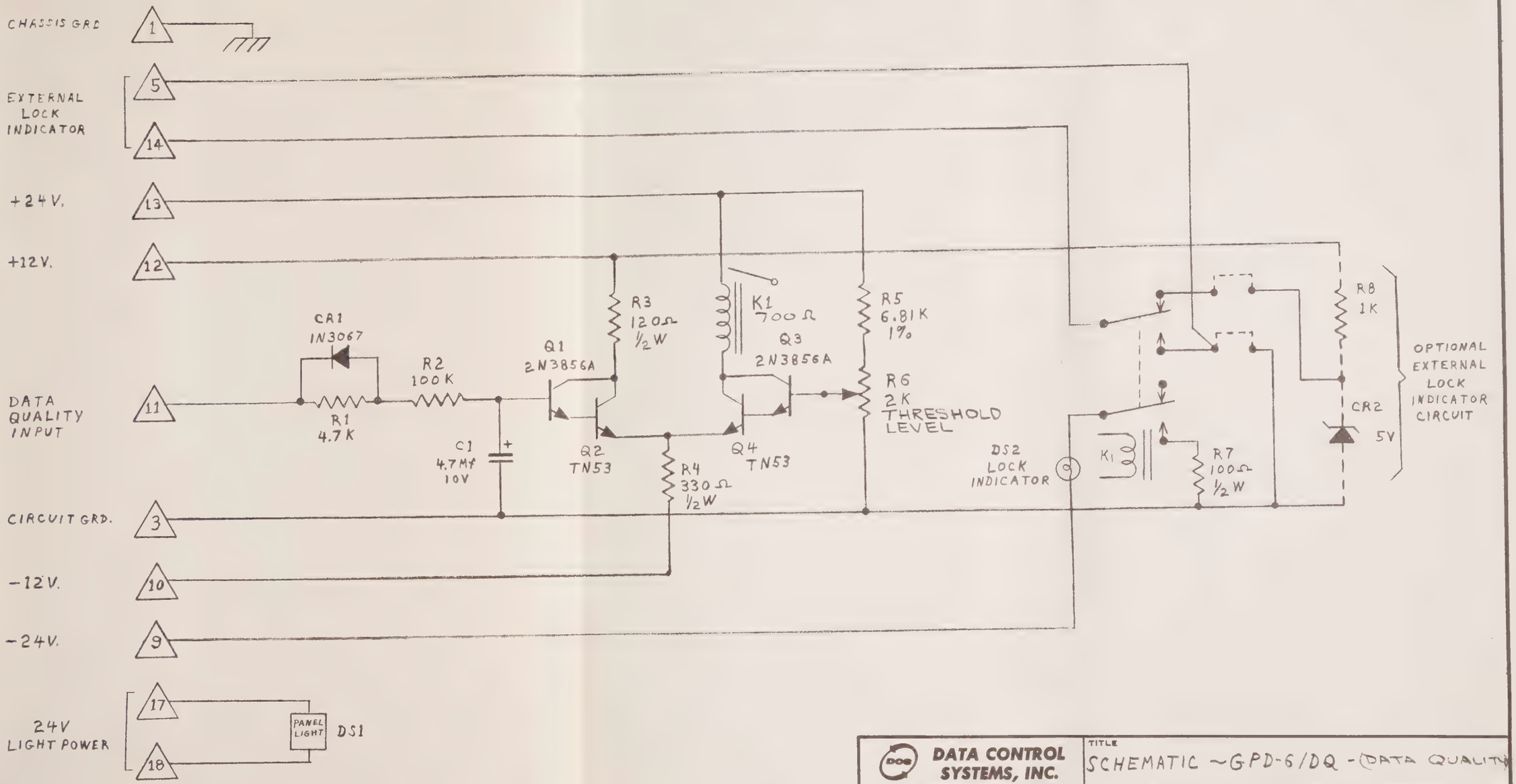
CA-015301 A

APP'D

PRODUCT | NEXT ASSEMBLY | QTY REQ'D

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B		REV.			

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY. / ASSY.



REF.	DESCRIPTION	QTY

PRODUCT	NEXT ASSEMBLY	QTY. / ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC ~GPD-6/DQ - DATA QUALITY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ✓

		DATE
DWN. HWM		2/9/68
CHKD. HWM		2/9/68
ENG. HWM		2/9/68
APP.		4/68
SCALE		

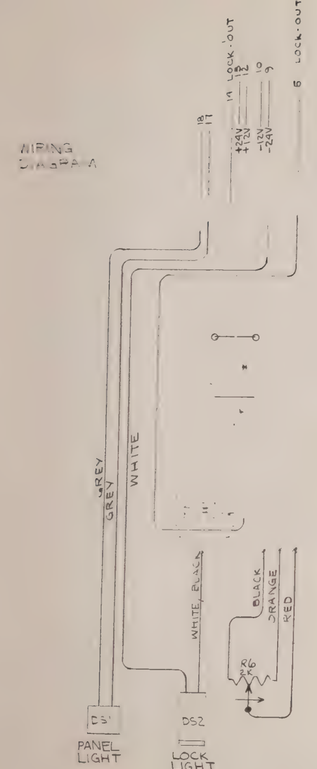
DO NOT SCALE DRAWING

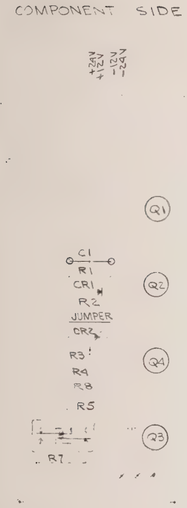
MAT'L

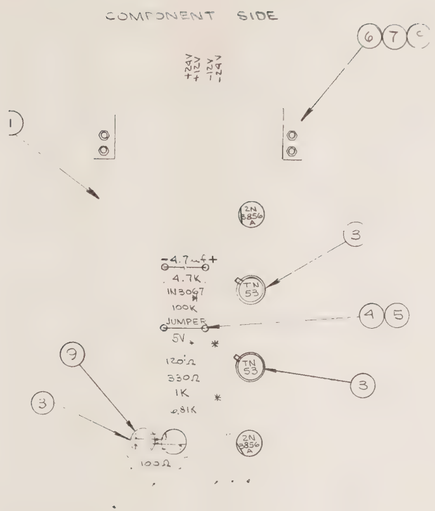
FINISH

BW - 017606 REV. A

SHEET







ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
1		CF-017605	BOARD FAB.	REF
2		BW-017606	SCHEMATIC	REF
	R1		RES, AB, CB, 1/4W, 10%, 1.7K	1
	R2		AB, CB, 1/4W, 10% 100K	1
	R3		AB, EB 1/2W 10% 120Ω	1
	R4		AB, FB, 1/2W, 10% 330Ω	1
	R5		ELECTRA, 1/4W, 1% 6.81K	1
	R6	GA2G024[illegible]52WA	AB, POT. 2K	1
	R7		AB, EB, 1/2W, 10%, 100Ω	1
*	R8		AB, CB, 1/4W, 10% 1K	1
	C1		CAP, [illegible]	1
	CR1		DIODE, 1N3067	1
*	CR2	SV5	DIODE, TRANSITRON OR EQUAL	1
	Q1		TRANS, GE 2N3866A	1
	Q2		SPRAGUE TN55	1
	Q3		GE 2N3866A	1
	Q4		SPRAGUE TN55	1
	K1	EA1A	RELAY, LEACH	1
3			TRANS PAD MILTON ROSS #10042	4
4			JUMPER #22 BUSS WIRE	A/R
5			TEFLON SLEEVING	A/R
	DS1	185-9830-[illegible]75	PANEL LIGHT, DIALCO	1
	DS2	507-23[illegible]-ED	LOCK INDICATOR, DIALCO	1
6		BD-[illegible]	BLOCK GUIDE	2
7		BD-[illegible]	PLATE WASHER	2
8		AS-826[illegible]	#[illegible]-40 PHIL.	4

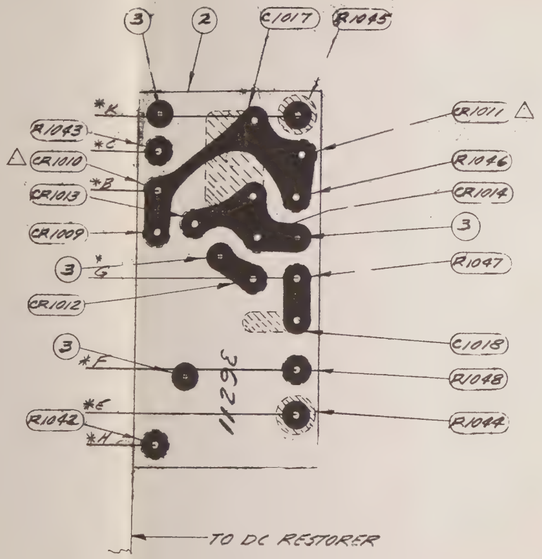
NOTE: * - OPTIONAL EXTERNAL LOCK INDICATOR CIRCUIT.

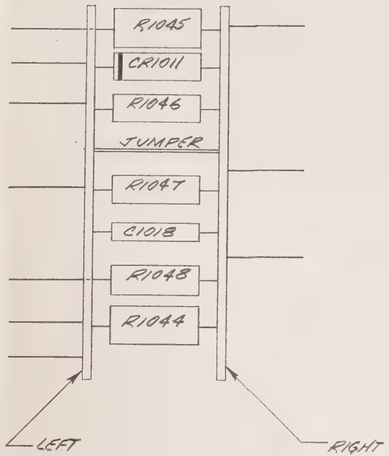
DATA CONTROL SYSTEMS, INC.	TITLE: BD. ASS'Y - GPD-6/DQ (DATA QUALITY)	
TOLERANCES - UNLESS OTHERWISE SPECIFIED DECIMAL - 3 PLACE ± .005 DECIMAL - 2 PLACE ± .010 FRAC. ± 1/64 ANG. ± 0°30' FLATNESS WITHIN /IN. FRACTIONAL HOLES -0, + 1/64 NOTE: BREAK ALL SHARP CORNERS .005"-.015"	DRAWN: J.E. HC 12-5-69 DATE 12/16/68 CHK'D: [illegible] 12-15-68 PROJ. ENG: [illegible] 12/15/69 CH. ENG: [illegible] 12/16/69 SCALE	DO NOT SCALE DRAWING MAT'L FINISH TA-017604 REV A

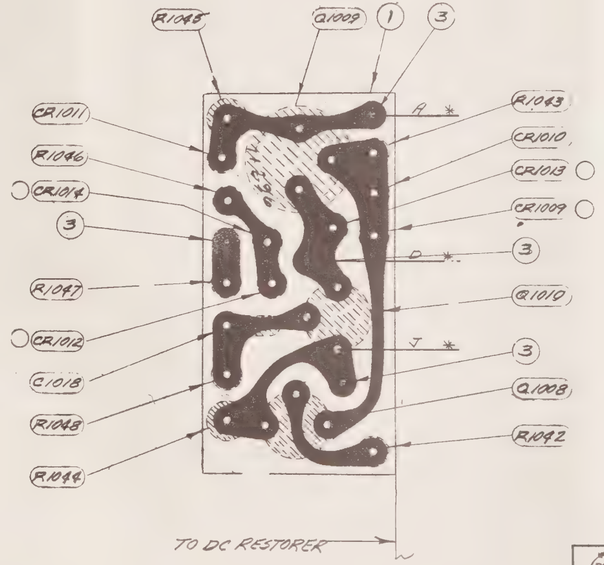
REV.	DESCRIPTION	DATE	DWN	CHK.	APP
B	ADD 3) REVISED LEADS 3) R1046 WAS 2K 3) Q1010 WAS 3658	1/30/67	RJW		
C	CA-3750 CHGD RES. VALUES	6/1/67		6/7/67	

T

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY. PER ASSY
1		BF-011296	UPPER PLUG-IN BOARD FAB	1
2		BF-011298	LOWER PLUG-IN BOARD FAB	1
3			JUMPER, #22 BUSS WIRE	A/F
	R1042		RES.AB,CB,1/4W,10% 150Ω	1
	R1043		10K	1
	R1044		ELECTRA,1/4W,1% 1K	1
	R1045		1.1K	1
	R1046		AB,CB,1/4W,10% 1.2K	1
	R1047		100	1
	R1048		1500	1
	Q1008		TRANS.,SE, 2N656A	1
	Q1009		" ME, 2N706	1
	Q1010		" GE, 2N858A	1
	C1017		CAP.,SPRAGUE TYPE 3K1	1
	C1018		" " " 3K2	1
	CR1009		DIODE,S.D., IN706	1
	CR1010		"	1
	CR1011		"	1
	CR1012		"	1
	CR1013		"	1
	CR1014		" IN751-A	1







NOTES:
* 1) LEADS TO BE EXTENDED APROX. (1) ONE INCH UNTIL MOUNTED TO DC RESTORER BOARD.
△ 2) DIODE TO BE MOUNTED WITH CATHODE TO LEFT
◯ 3) DIODE TO BE MOUNTED WITH CATHODE TO RIGHT

REF.	DESCRIPTION	QTY.

GPD-6	GA-015166	1
FIRST PRODUCT	NEXT ASSEMBLY	QTY. ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE: ASSY, PLUG IN, DC RESTORER

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN .001 IN.
FRACTIONAL HOLES -0. + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED 125

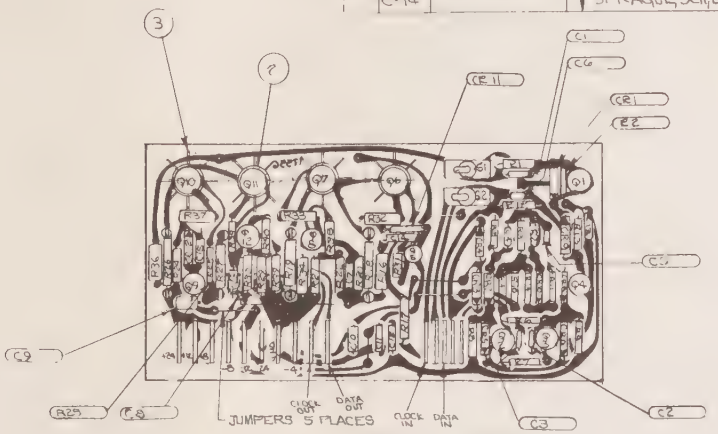
DWN. RJW 1/30/67
CHKD. [illegible] 6/7/67
ENG. [illegible]
APP. [illegible]
SCALE ~

DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

TA-015723 REV. C
SHEET

REV	DATE	DESCRIPTION	BY
B	3/27/68	I&E REVISED DWG.	JP
C	9/9/68	I&E INTERCHANGED POSITION OF C8 & C13	JP

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY
	R40		RES, AB, CB, ¼W, 10% 100Ω	1
	C-1		CAP, ERIE, 831 10% 47pf	1
	C-2		15pf	1
	C-3		15pf	1
	C-4		150pf	1
	C-5		68pf	1
	C-6		22pf	1
	C 7		SPRAGUE, 5C11, 25V .47μf	1
	C 8		.47μf	1
	C 9		5C13, 25V 1μf	1
	C-10		1μf	1
	C 11		1μf	1
	C-12		1μf	1
	C-13		1μf	1
	C-14		SPRAGUE, 5C11, 25V, .47μf	1



ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY
	C 5		CAP, SPRAGUE, 5C11, 25V, 47μf	1
	Q-1		TRANS, FAIRCHILD, 2N4250	1
	Q-2			1
	Q 3			1
	Q-4			1
	Q-5		2N3638	1
	Q-6	SEE NOTE #1	SPRAGUE TQ59	1
	Q-7			1
	Q-8		FAIRCHILD 2N3638	1
	Q 9			1
	Q-10	SEE NOTE #1	SPRAGUE TQ59	1
	Q 11			1
	Q 12		FAIRCHILD 2N3638	1
	S-1		SWITCH TORBAL SP-5	1
	S2			1
3		HEATSINK	NF-207 WAKEFIELD	4

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY
1	~	CF-017556	BD. FAB, CONVERTER	1
2	~	#A10068	TRANS, PAD, ROSS	6
	CR-1		DIODE CONT. DEV, IN3067	1
	CR-2			1
	CR-3			1
	CR-4			1
	CR-5			1
	CR-6			1
	CR-7			1
	CR-8			1
	CR-9			1
	CR-10			1
	CR-11		IN716	1
	CR-12			1
	R 1		RES, AB, CB ¼W, 10% 2.2K	1
	R-2		12K	1
	R-3		470Ω	1
	R-4		1.2K	1
	R 5		2.2K	1
	R-6		4.7K	1
	R 7		4.7K	1
	R-8		120K	1
	R 9		120K	1
	R-10		1.2K	1
	R 11		1K	1
	R 12		2.2K	1
	R-13		12K	1
	R 14		1.2K	1
	R-15		1. 8K	1
	R 17		AB EB, 10% ½W, 47Ω	1
	R-18		MEPCO, P-20, 5%, 2½W, 300Ω	1
	R-19		1% 90.9Ω	1
	R-20		AB, CB, ¼W 10% 6.8K	1
	R-21		ELEC, MFSC-D, 1% 1.96 K	1
	R 22		2.61K	1
	R-24		AB, CB, ¼W, 10% 1.8K	1
	R-25		½W, 10% 47Ω	1
	R 26		MEPCO, P120, 5%, 2½W, 200Ω	1
	R-27		1% 90.9Ω	1
	R28		AB, CB, ¼W, 10% 6.8K	1
	R-29		ELEC, MFSC-D, 1% 1.96K	1
	R30		2.61K	1
	R31		AB, CB ¼W, 10% 100Ω	1
	R32		100Ω	1
	R 33		100Ω	1
	R 34		1K	1
	R 35		100Ω	1
	R 36		100Ω	1
	R 37		100Ω	1
	R 38		100Ω	1
	R 39		1K	1

NOTE: 1) 2ND CHOICE MOTOROLA 2N3133

REF	DESCRIPTION	QTY

GPD-6D	DA-015271	1
PRODUCT	NEXT ASSEMBLY	

DATA CONTROL SYSTEMS, INC.

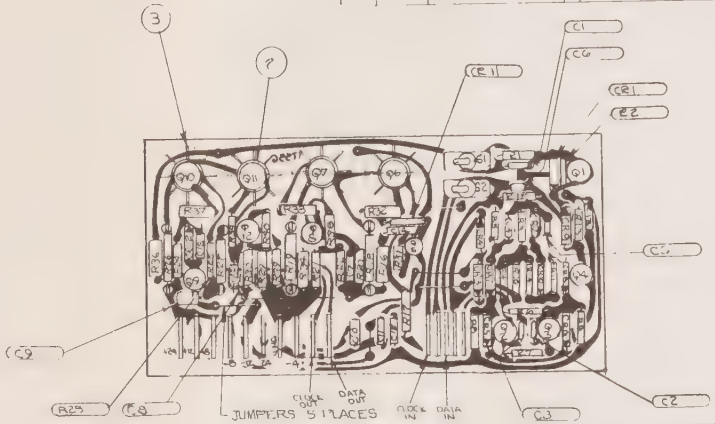
BD. ASSY CODE CONVERTER

DO NOT SCALE DRAWING

CA-017557 C

REV	DATE	DESCRIPTION	
B	3/27/68	I&E REVISED DWG.	
C	5/3/68	I&E INTERCHANGED POSITION OF C8 TO C6	

ITEM	SYMBOL	DWG. NO	DESCRIPTION	QTY ASSY
	R40		RES, AB, CB, ¼W, 10% 100Ω	1
	C-1		CAP, ERIE, 831 10% 47pf	1
	C-2		15pf	1
	C-3		15pf	1
	C-4		150pf	1
	C-5		68pf	1
	C-6		22pf	1
	C-7		SPRAGUE, 5C11, 25V .47μf	1
	C-8		.47μf	1
	C-9		5C13, 25V 1μf	1
	C-10		1μf	1
	C-11		1μf	1
	C12		1μf	1
	C-13		1μf	1
	C-14		SPRAGUE, 5C11, 25V, .47μf	1



ITEM	SYMBOL	DWG. NO	DESCRIPTION	QTY
	C-15		CAP, SPRAGUE, 5C11, 25V, 47μf	1
	Q-1		TRANS, FAIRCHILD, 2N4250	1
	Q-2			1
	Q-3			1
	Q-4			1
	Q-5		2N3633	1
	Q-6	SEE NOTE #1.	SPRAGUE TQ59	1
	Q-7			1
	Q-8		FAIRCHILD 2N3638	1
	Q-9			1
	Q-10	SEE NOTE #1	SPRAGUE TQ59	1
	Q-11			1
	Q-12		FAIRCHILD 2N3638	1
	S-1		SWITCH TORBAL SP-5	1
	S-2			1
3		HEATSINK	NF-207 WAKEFIELD	4

ITEM	SYMBOL	DWG. NO	DESCRIPTION	QTY

NOTE: 1) 2ND CHOICE MOTOROLA 2N3133

ITEM	SYMBOL	DWG. NO	DESCRIPTION	QTY ASSY
1	~	CF-017556	BD. FAB, CONVERTER	1
2	~	#A10068	TRANS, PAD, ROSS	6
	CR-1		DIODE CONT. DEV, IN3067	1
	CR-2			1
	CR-3			1
	CR-4			1
	CR-5			1
	CR-6			1
	CR-7			1
	CR-8			1
	CR-9			1
	CR-10			1
	CR-11		IN716	1
	CR-12			1
	R-1		RES, AB, CB ¼W, 10% 2.2K	1
	R-2		12K	1
	R-3		470Ω	1
	R-4		1.2K	1
	R-5		2.2K	1
	R-6		4.7K	1
	R-7		4.7K	1
	R-8		120K	1
	R-9		120K	1
	R-10		1.2K	1
	R-11		1K	1
	R-12		2.2K	1
	R-13		12K	1
	R-14		1.2K	1
	R-16		1.8K	1
	R-17		AB, EB, 10%, ½W, 47Ω	1
	R-18		MEPCO, PI20, 5%, 2½W, 200Ω	1
	R-19		1% 90.9Ω	1
	R-20		AB, CB, ¼W 10% 6.8K	1
	R-21		ELEC. MFSC-D 1% 1.96 K	1
	R-22		2.61K	1
	R-24		AB, CB, ¼W, 10% 1.8K	1
	R-25		½W, 10% 47Ω	1
	R-26		MEPCO, PI20, 5%, 2½W, 200Ω	1
	R-27		1% 90.9Ω	1
	R28		AB, CB, ¼W, 10% 6.8K	1
	R29		ELEC, MFSC-D, 1% 1.96K	1
	R30		2.61K	1
	R31		AB, CB ¼W, 10% 100Ω	1
	R32		100Ω	1
	R33		100Ω	1
	R34		1K	1
	R35		100Ω	1
	R36		100Ω	1
	R37		100Ω	1
	R38		100Ω	1
	R39		1K	1

REF	DESCRIPTION	QTY

GPD-6D	DA-015271	1
PROJECT	NEXT ASSEMBLY	

DATA CONTROL SYSTEMS, INC.

TITLE: BD. ASS'Y CODE CONVERTER

DO NOT SCALE DRAWING

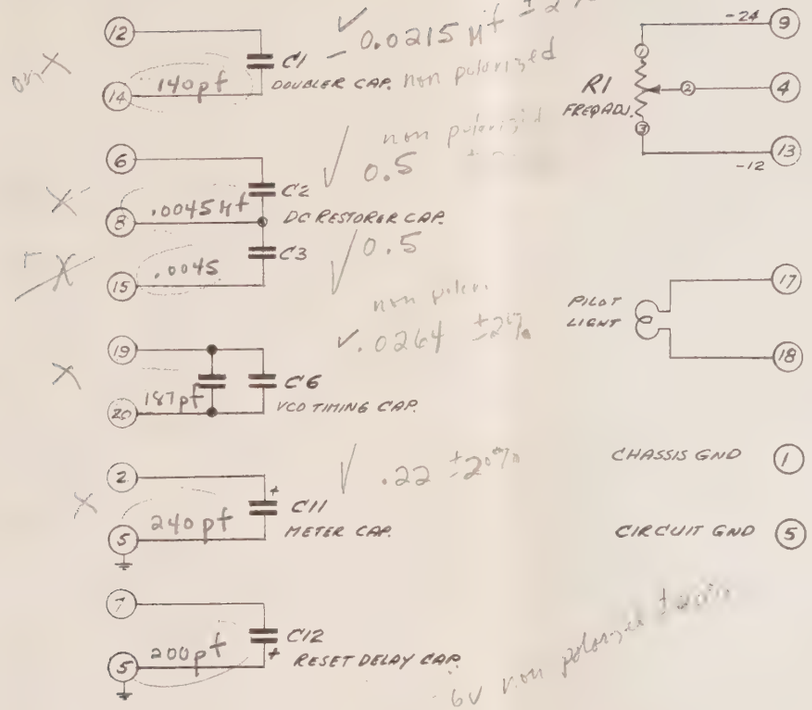
SIZE: C | CA - 017357 | REV: C

SHEET 1 TO 1

GPD-6/F
REF. TU.

REVISIONS					
SYM.	DESCRIPTION	DATE	BY	CHK'D	APP'D
B	R+E Change - Added Low Channel 2 pos.	3/11/67	H W M		

BOARD #1
LOWER

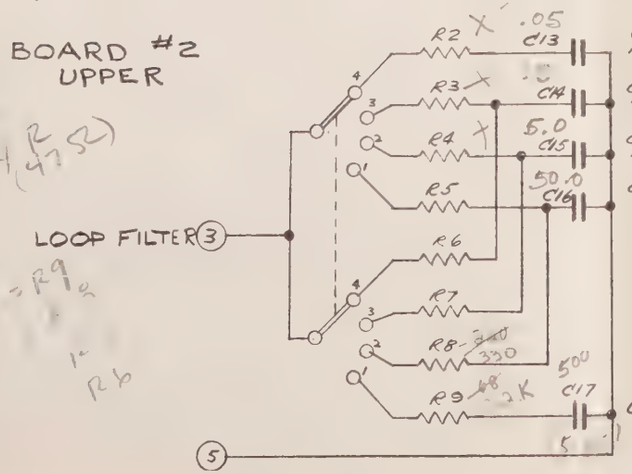


FLCO Conn on Left-hand side
1 on TOP
20 on BOTTOM

SERIES 100 (LOWER BOARD)

SERIES 200 (UPPER BOARD)

BOARD #2
UPPER



Position	High Channels	Low Channels
4	1% WIDE	2 1%
3	.3%	1 .3%
2	.1%	
1	.03% NARROW.	

C/10000 500pf
C/1000 .005Mf
C/100 .05Mf
C/10 .5Mf

High Channels
Loop Filter
R2 THRU R5 = 47Ω
R6 = 2.2k
R7 = 680Ω
R8 = 220Ω 330
R9 = 68Ω 2.2K

Low Channels
Two position Loop filter.
Resistors R2, R3, R6 and R7 used

Notes:
1) RES. ARE MF, CB 1/4 W, 10% UNLESS OTHERWISE SPECIFIED.
2) ALL OTHER COMPONENTS ARE FREQUENCY SENSITIVE, SEE FINAL ASSY.

GPD-6/F

DATA CONTROL SYSTEMS, INC.	TITLE: SCHEMATIC, REF. TUNING UNIT		
TOLERANCES: UNLESS OTHERWISE SPECIFIED DECIMAL - 3 PLACE ± .005 DECIMAL - 2 PLACE ± .010 FRAC. ± 1/64 ANG. ± 0°30' FLATNESS WITHIN ~ IN. FRACTIONAL HOLES -0, + 1/64 NOTE: BREAK ALL SHARP CORNERS .005"-.015"	DWN. RE DATE 10/27/66 CHK'D RTW " 12/66 PROJ. ENG. " 11/4/66 CH. ENG. RT " 12/66 SCALE ~	DO NOT SCALE DRAWING MAT'L FINISH	
	BW-015307	REV. B	

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-2824-CHG'D. SYMBOLS & BOARD LOCATION	9/16/65			
C	CA-3190- CHGD R3112 FROM 2.7K TO 2.2K.	2/29/66			
D	CA-3190-1 - R1310 WAS 1.2K	3/23/66			
E	CA-3749 - CHG DIODE VALUES	5/29/67			
F	CA-3849-1 CHG CAP VALUES C1311, 1313	9/15/67			

REF.	DESCRIPTION	QTY

-12V J1300-5

-4V J1300-8

VCO J1300-12

NRZ DATA OUT J1300-17

VCO J1300-13

DATA J1300-18

DATA J1300-16

GRD J1300-7

+12V J1300-2

TO CODE SW "A2", "A3", "A4" J1300-15 P1500-15

TO CODE SW "C3" J1300-14

R1315 2.7K
R1313 2.7K
R1314 22K
R1312 2.2K
R1305 1.0K
R1306 1.0K
R1302 1.8K
R1301 220Ω
R1303 1.2K
R1310 470Ω
R1316 820Ω
R1309 4.7K
R1304 4.7K
R1317 4.7K
R1307 120K
R1308 120K
R1311 1.0K
R1318 1.0K

C1316 1.0μf
C1317 1.0μf
C1318 1.0μf
C1319 1.0μf
C1314 15μμf
C1301 15μμf
C1305 15μμf
C1306 15μμf
C1302 47 μμf
C1303 47 μμf
C1304 68μμf
C1315 1.0μf

Q1305
Q1304
Q1301
Q1302
Q1303
Q1306

CR1310 CTP 700A
CR1303 470K
CR1307
CR1311
CR1309
CR1305
CR1306
CR1301
CR1302 470K
CR1304 IN191
CR1308 IN191
CR1312 IN191

"0" "A" "1"

RG SG SG

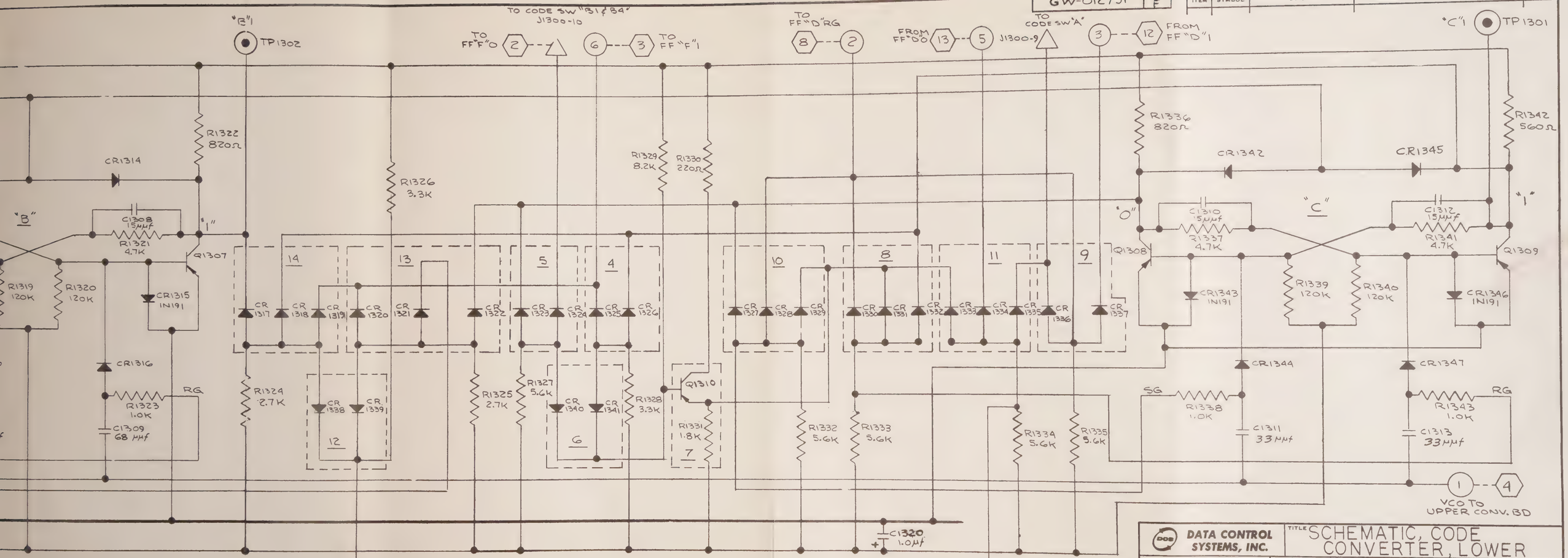
1 2 3

TP1301 TP1302

1 2 3 4 5 6 7

SKETCH SHOWING LOCATION & IDENTIFICATION OF TERMINALS & TEST POINTS.

NOTE:
1) ALL DIODES CGD 1032 UNLESS OTHERWISE NOTED.
2) ALL TRANSISTORS GM592-A UNLESS OTHERWISE NOTED.



3) ○ TERMINALS ON CODE CONVERTER, LOWER BD
4) ○ TERMINALS ON CODE CONVERTER, UPPER BD
5) REF. SCHEMATIC TW-012726
6) REF. ASSY TA-011773
7) REF. BLOCK DIAGRAM DB-013312
8) △ ELCO CONN. TO MOTHER BD-1500

GW-012731	F			
ITEM	SYMBOL			

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, CODE CONVERTER, LOWER

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ / IN.
FRACTIONAL HOLES -0 + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN. DH		9/18/69
CHKD.		11/15/65
ENG.		9/14/65
APP.		9/14/65
SCALE 2		

DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

GW-012731 REV. F
SHEET

GPS-5	~	~
FIRST PRODUCT	NEXT ASSEMBLY	QTY. ASSY.

SECTION VII

DIFFERENCE DATA

7-1. SCOPE.

7-2. This section contains difference data sheets for the GPD-6. All variations of the basic equipment are documented herein.

DEPT. 29-52-20